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MS-7816

Intel -SharkBay plamform Z87

ATX

Ver: 12(243.84x304.8)

CPU:

Haswell LGA1150

System Chipset:

Lynx Point Z87

Onboard Chip:

HD Audio Codec:ALC892

LAN-RTL8111E

SIO:Nuvoton 6779D

Flash ROM: SPI 64 MB & SPI 128 MB (H87&B85)

Main Memory:

DDRIII (1066/1333/1600MHz) * 4 (Dual Channel)

ACPI:

UPI

PWM:

UP1649 6 Phase

Expansion Slots:

Other:

SATA3.0 x6(PCH)
REAL USB2.0 *6
FRONT USB2.0 *4(B85 Disable 2 port)
REAL USB3.0 *2
FRONT USB3.0 *2

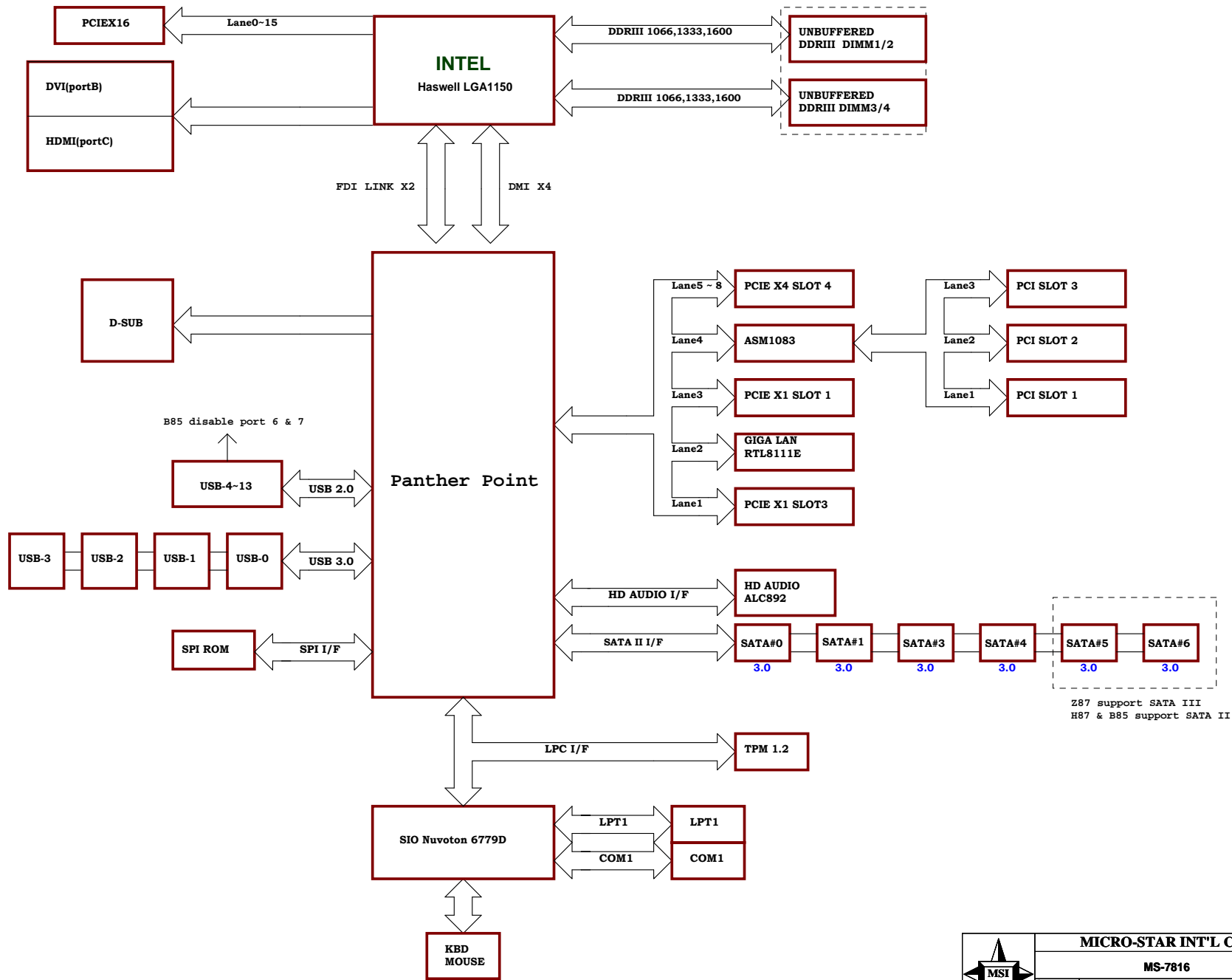
PCI Express (X16) Slot * 1

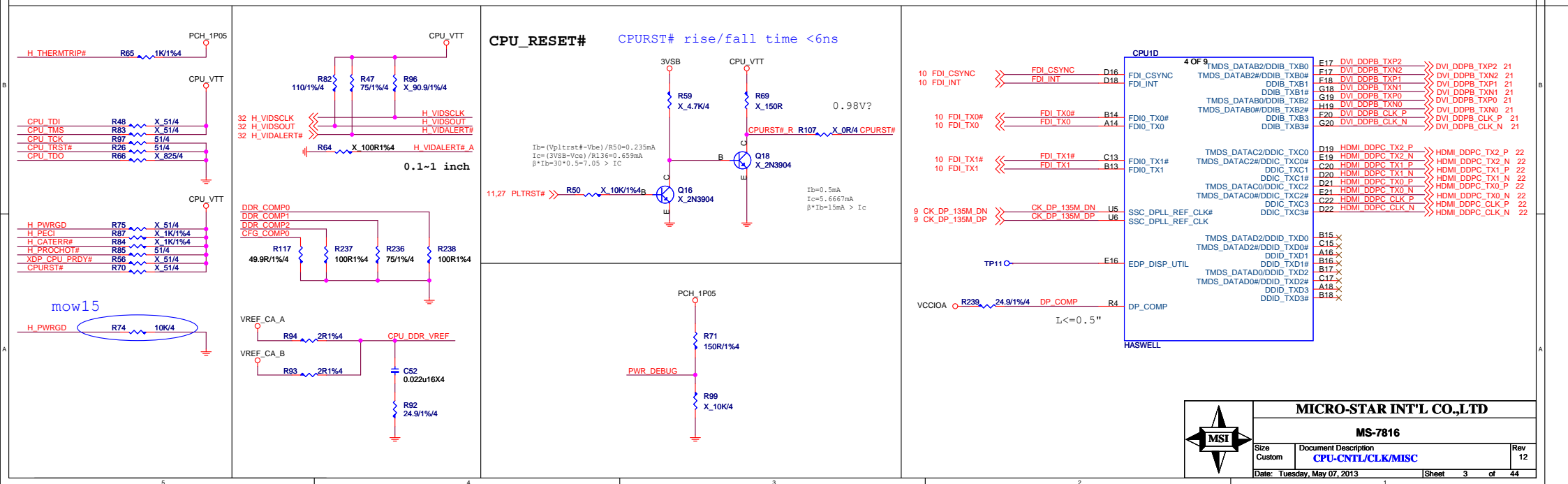
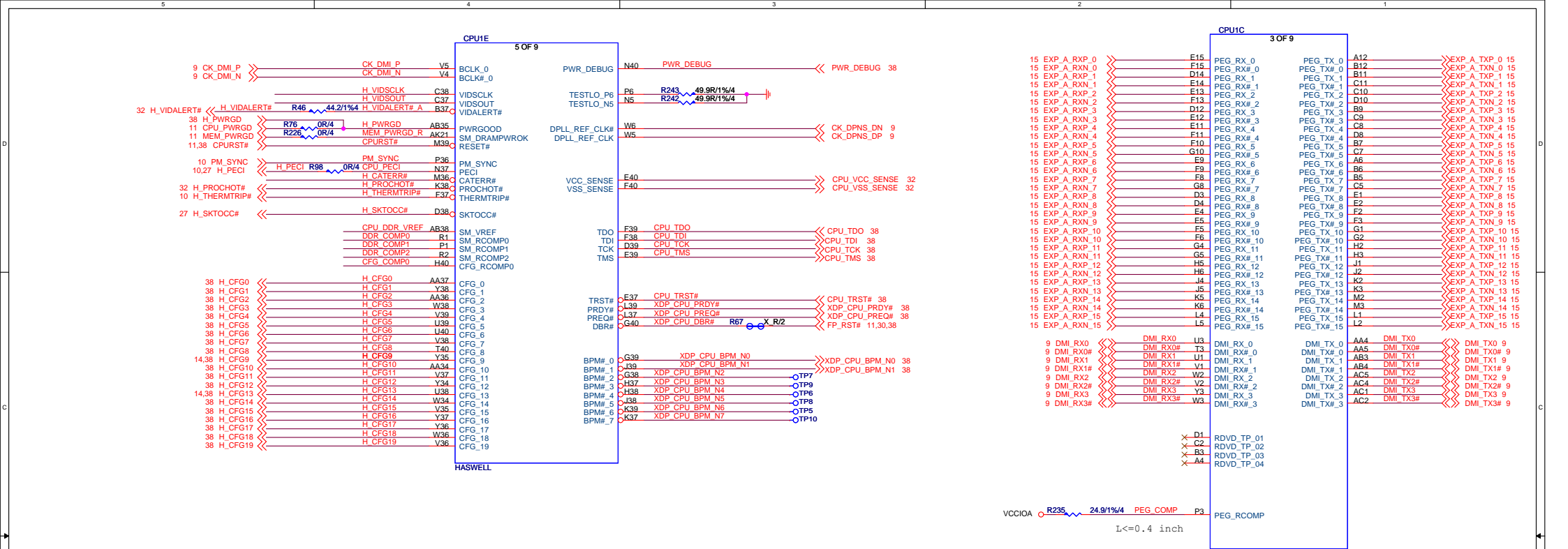
PCI Express (X1) Slot * 2

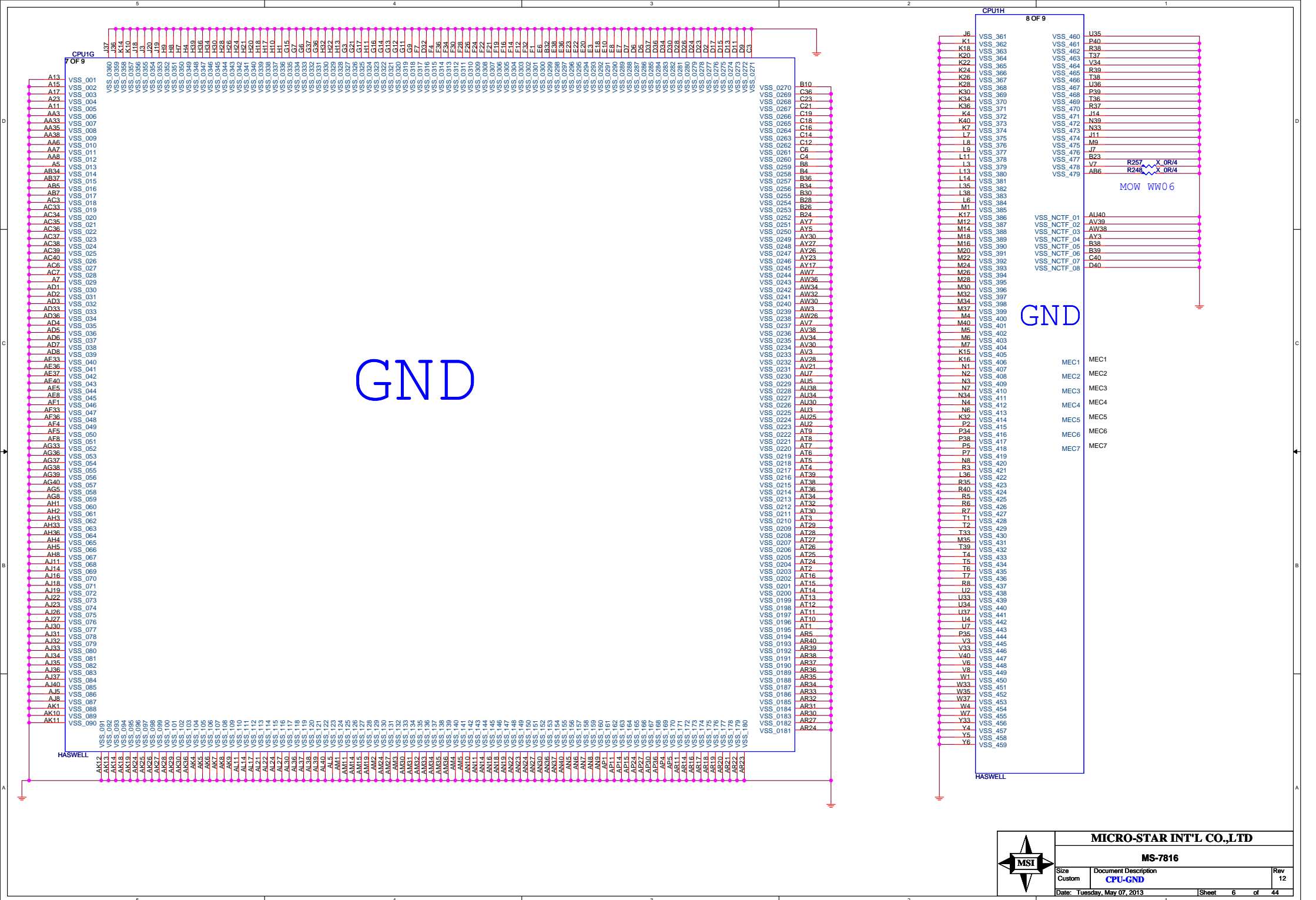
PCI Express (X4) Slot * 1

PCI Slot * 3

MS-7816 Block Diagram







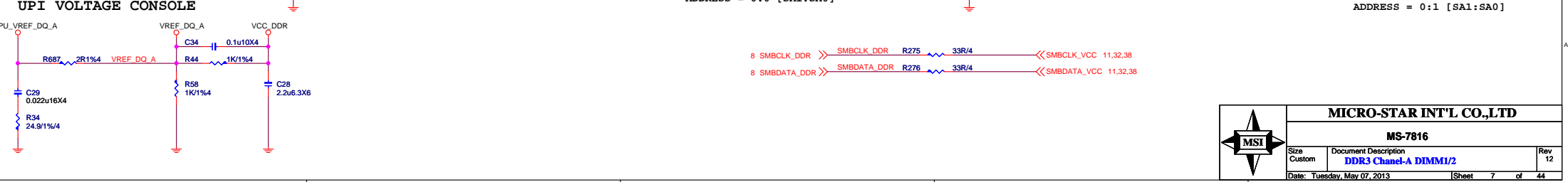
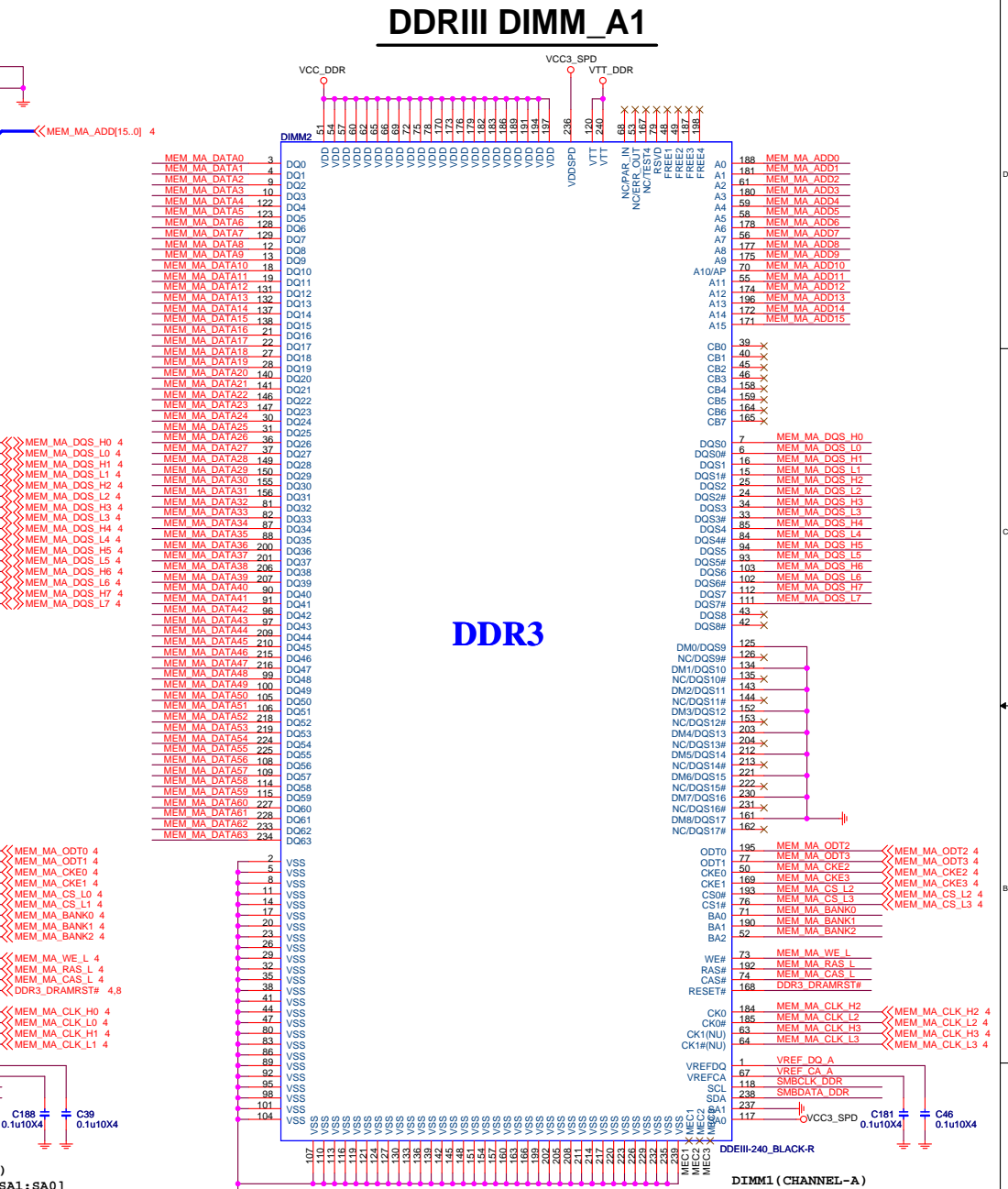
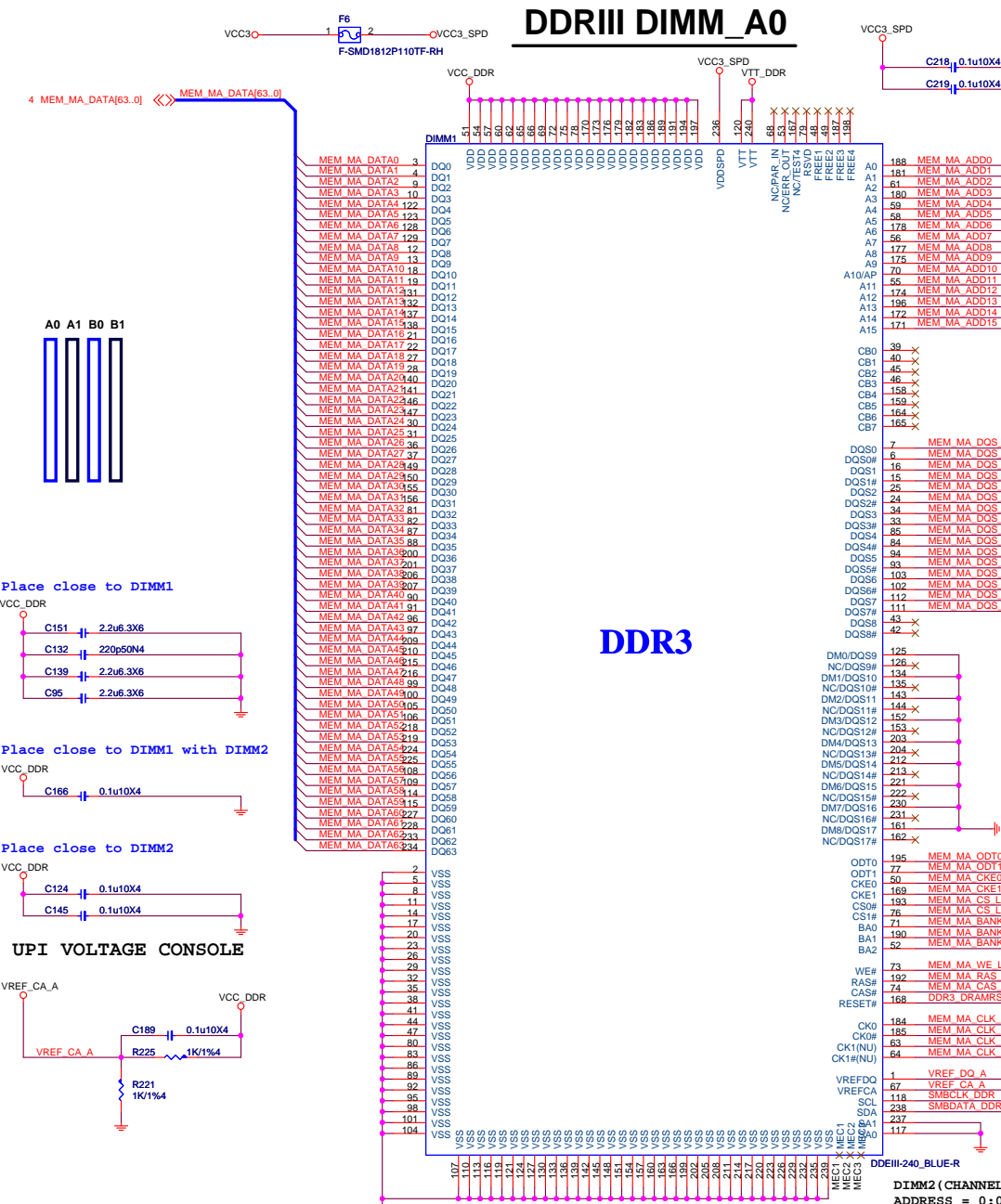
MICRO-STAR INT'L CO.,LTD

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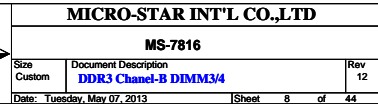
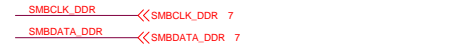
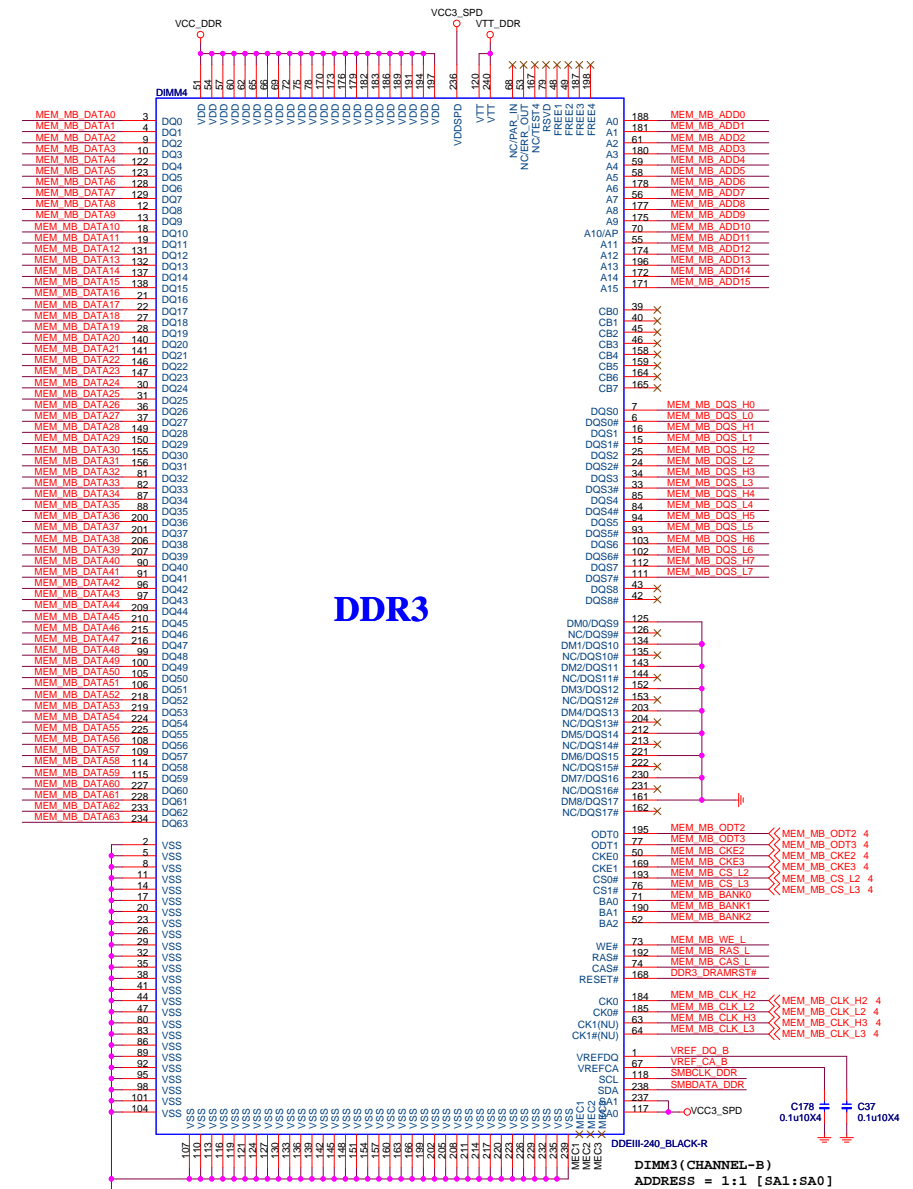
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DDR3 DIMM A0

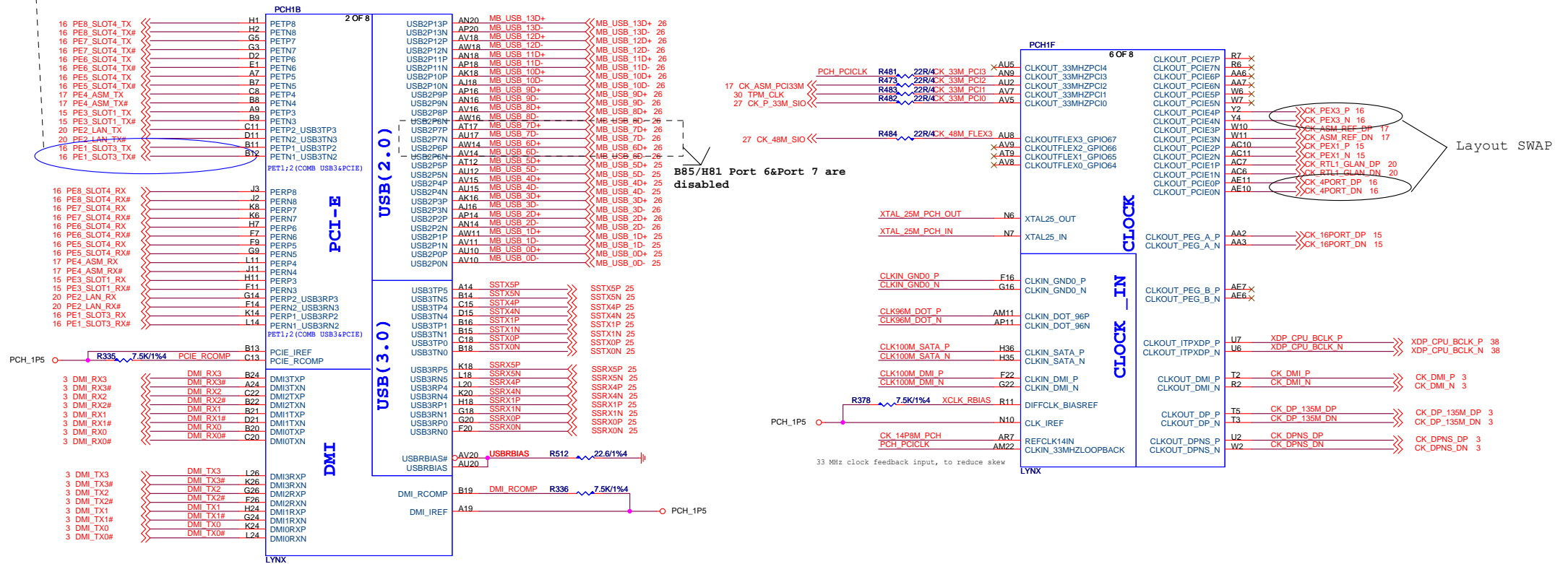
DDR3 DIMM A1



DDRIII DIMM_B1



PCIE Port 0 requires a link corresponding to the PCIE Device.(Because the PCIe port0 then the Device to open the Enable / Disable option in the bios interface.)



no clock gen pull down

CLK96M DOT P R509 10K/4
CLK96M DOT N R508 10K/4
CLK100M SATA P R372 10K/4
CLK100M SATA N R379 10K/4

CLKIN_GND0_P R330 10K/4
CLKIN_GND0_N R329 10K/4
CLK100M DMI N R331 10K/4
CLK100M DMI P R332 10K/4

CK_14P8M_PCH R510 10K/4

EMI

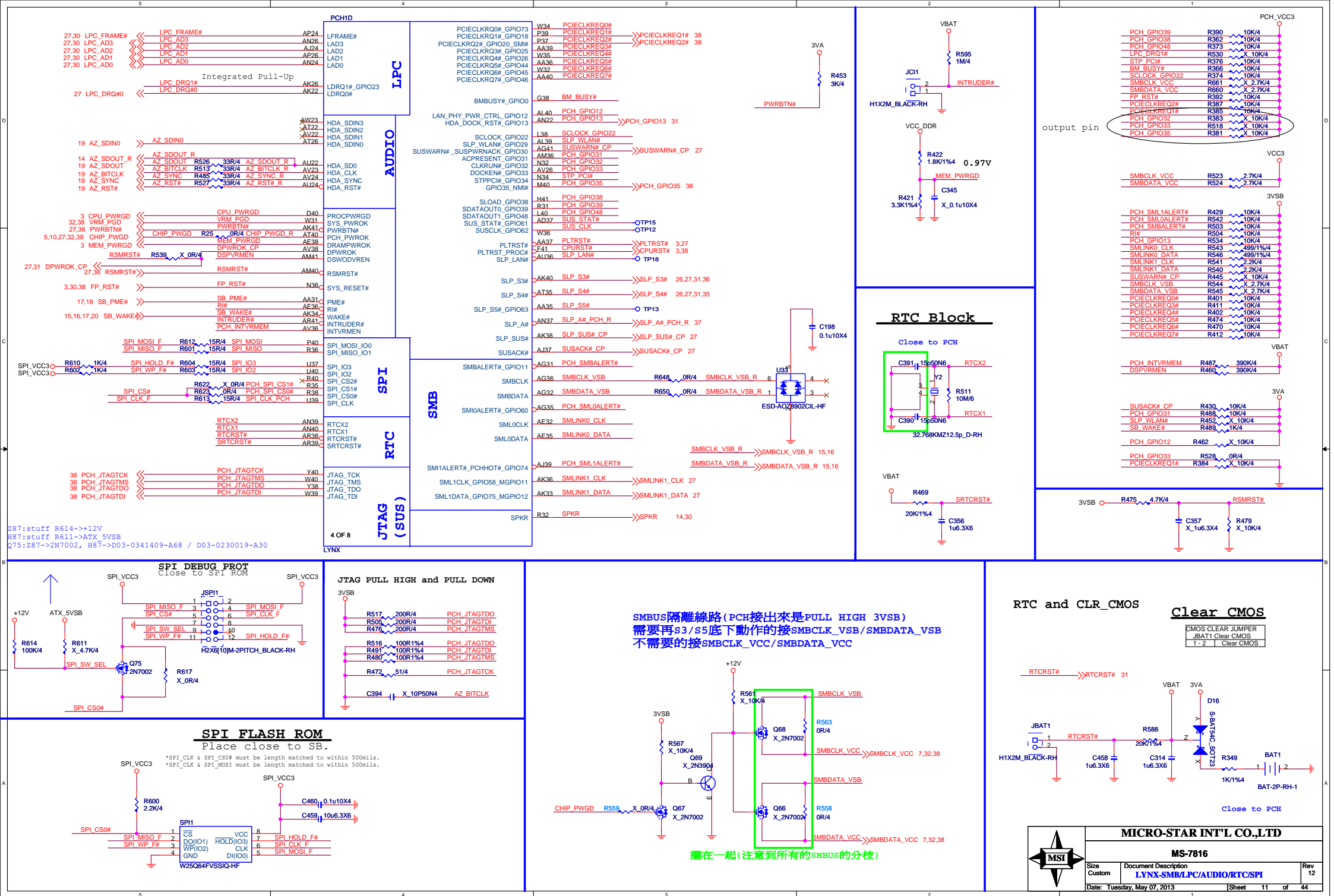
PCH_PCLK C369 X 10P50N4
CK_ASM_PCLK C361 X 10P50N4
TPM_CLK C385 X 10P50N4
CK_P_33M_SIO C384 X 10P50N4
CK_48M_SIO C386 X 10P50N4



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AF25 ;AD25 DT CRB0.7 ASW POWER

(Internal) 1.29A+(External)1.12A=2.41A

POWER

AG1 DT CRB0.7 VCC3 POWER

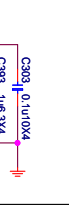
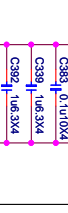
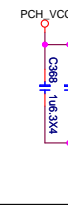
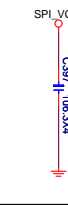
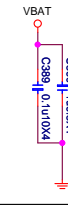
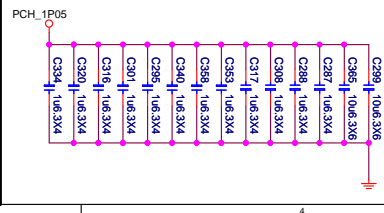
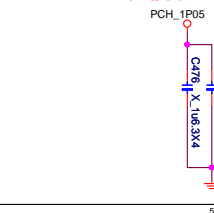
(Internal) 0.261A+(External)0.261A=0.532A

PCH decoupling cap

VCC3 0.21A
3VA 0.015A
VBAT 6uA
3VSB 0.261A
VCC1_5 0.249A
PCH_1P05 6A

Backside for V14,U12,T16,V16

unstuff



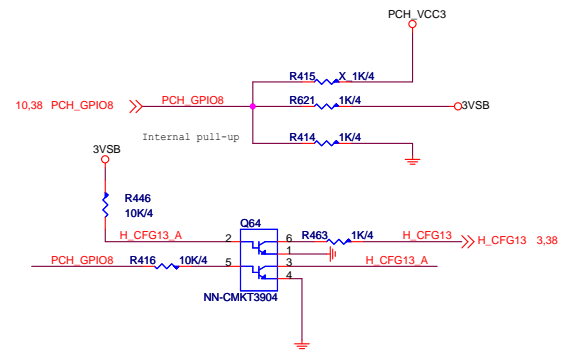
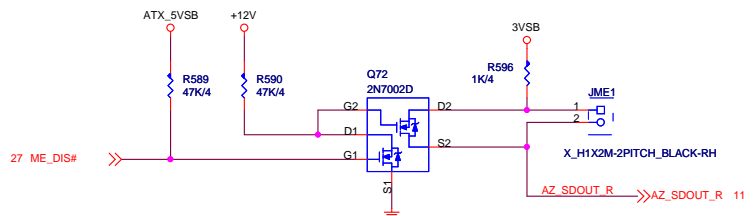
MICRO-STAR INT'L CO.,LTD		
MS-7816		
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11,30 SPKR << SPKR R391 X 8.2K/4

Internal pull-DOWN

SPKR
Default Mode:
Internal weak Pull-down.

No Reboot Mode with TCO Disabled:
Connect to Vcc3_3 with 8.2k-10k Ohm weak pullup resistor.

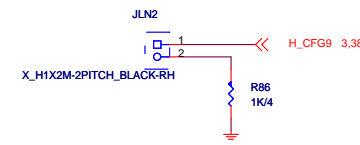


10 PCH_GPIO55 >> PCH_GPIO55 R461 X 4.7K/4

Internal pull-up

GPIO55
Default Mode:
Internal pull-up.

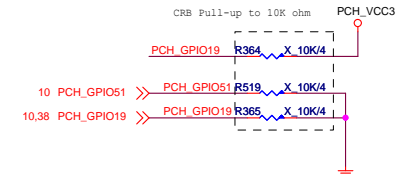
Top Block Swap Mode:
Connect to ground with 4.7k Ohm weak pulldown resistor.



10 PCH_GPIO53 >> PCH_GPIO53 R486 X 1K/4

GPIO53
Connect to ground with 1k Ohm pull-down resistor.

For Sx power Cycling May Fail Due to SVID Logic Race Condition Within the Processor



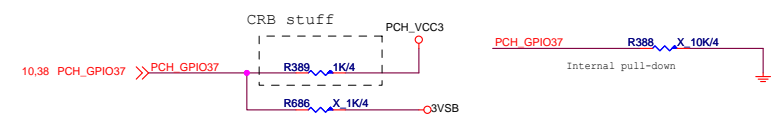
Default (SPI):
Left both SATA1GP/GPIO19 and GPIO51 floating.
No pull up required.

Boot from PCI:
Connect SATA1GP/GPIO19 to ground with 1k Ohm pull-down resistor.
Leave GPIO51 Floating.

Boot from LPC:
Connect both SATA1GP/GPIO19 and GPIO51 to ground with 1k Ohm pull-down resistor.

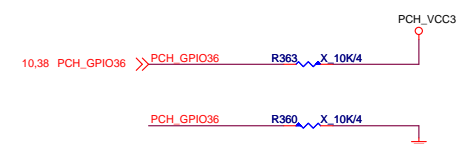
BOOT DEVICE	GPIO51	GPIO19
LPC	0	0
SPI	1	1

Default



Enable TLS:
Pull up with 1k Ohm to VccSus3.3.

Default (Disable TLS):
Leave NC. Internal pull down.



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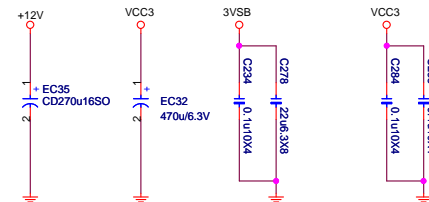
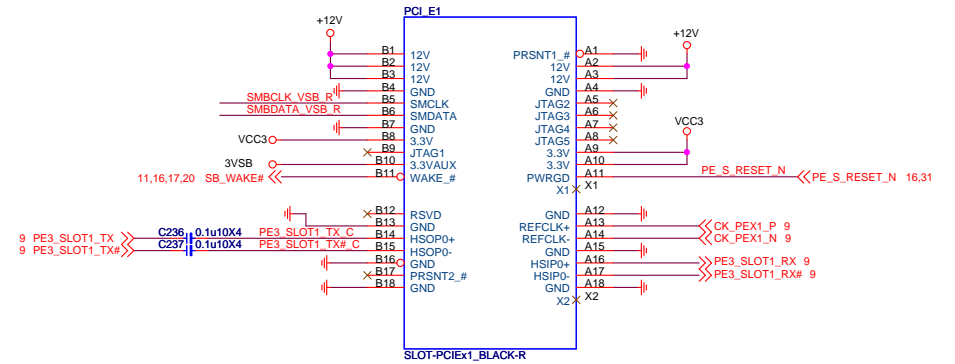
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Size Custom Document Description **LYNX-Strap** Rev 12

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11,16 SMBCLK_VSB_R
11,16 SMBDATA_VSB_R

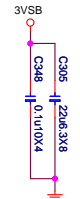
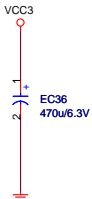
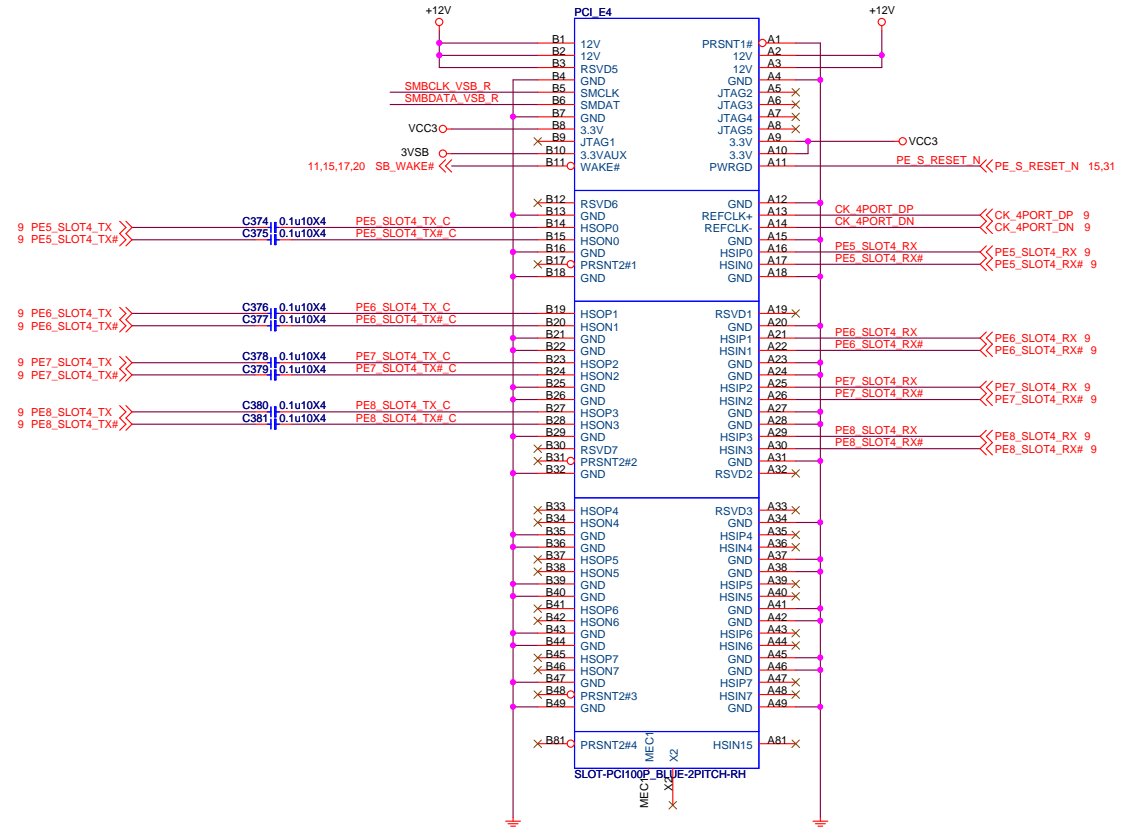
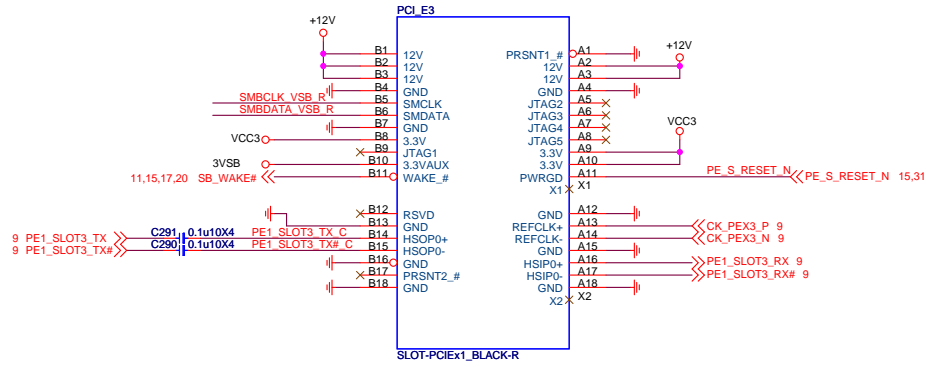
SMBCLK_VSB_R
SMBDATA_VSB_R



11,15 SMBCLK_VSB_R
11,15 SMBDATA_VSB_R

SMBCLK_VSB_R
SMBDATA_VSB_R

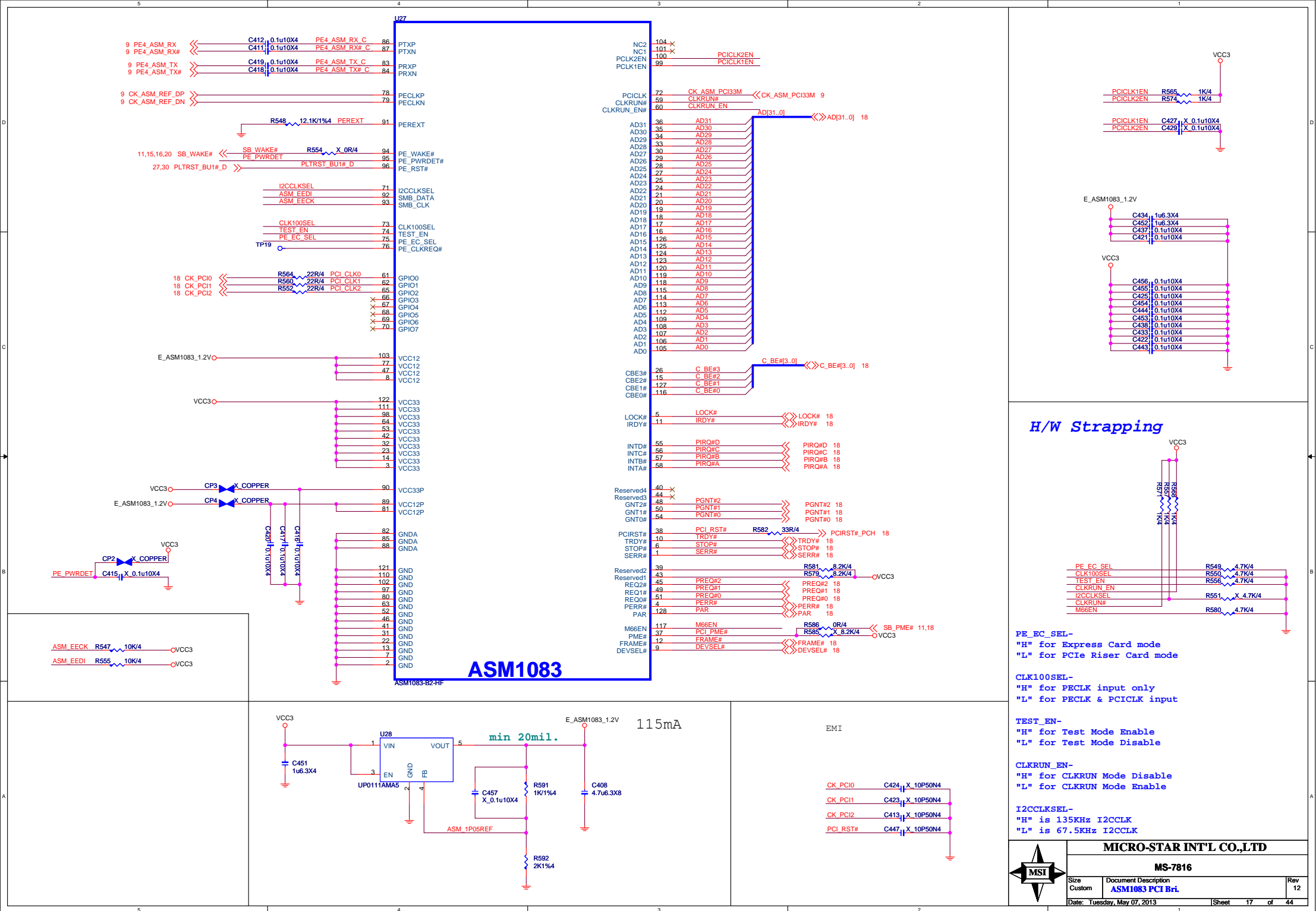
PCI_Express X4 Slot

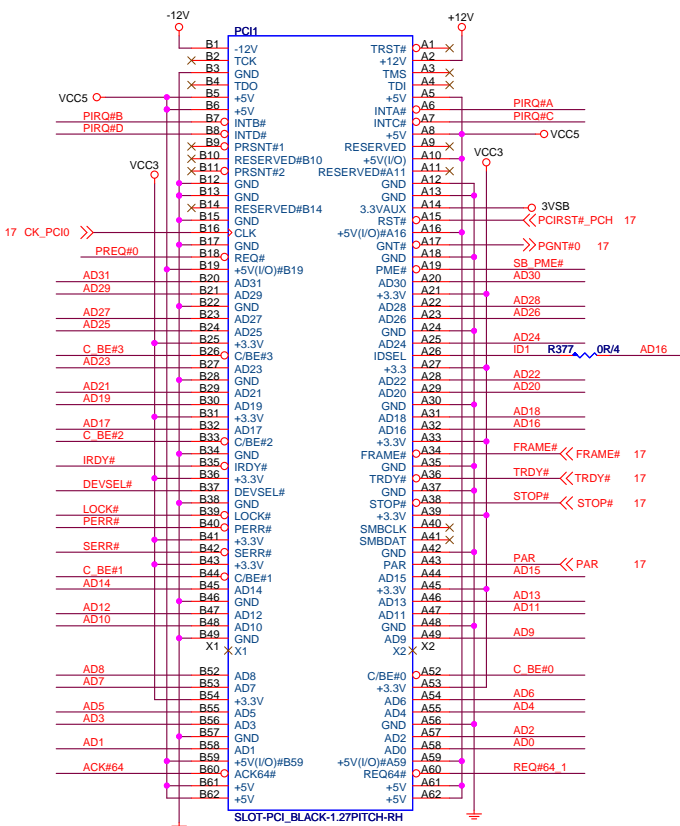


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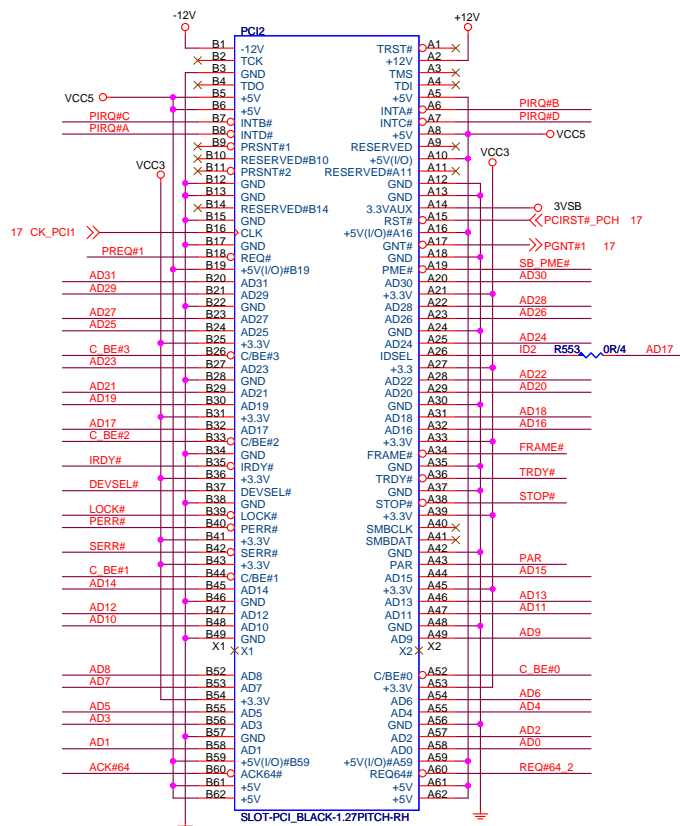
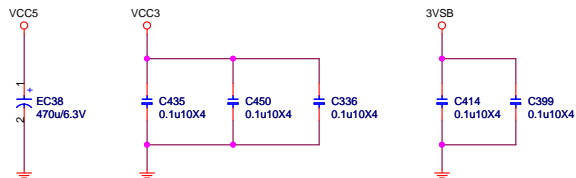
Size	Document Description	Rev
Custom	PCIE3(X1) & PCIE4(X4) Slots	12
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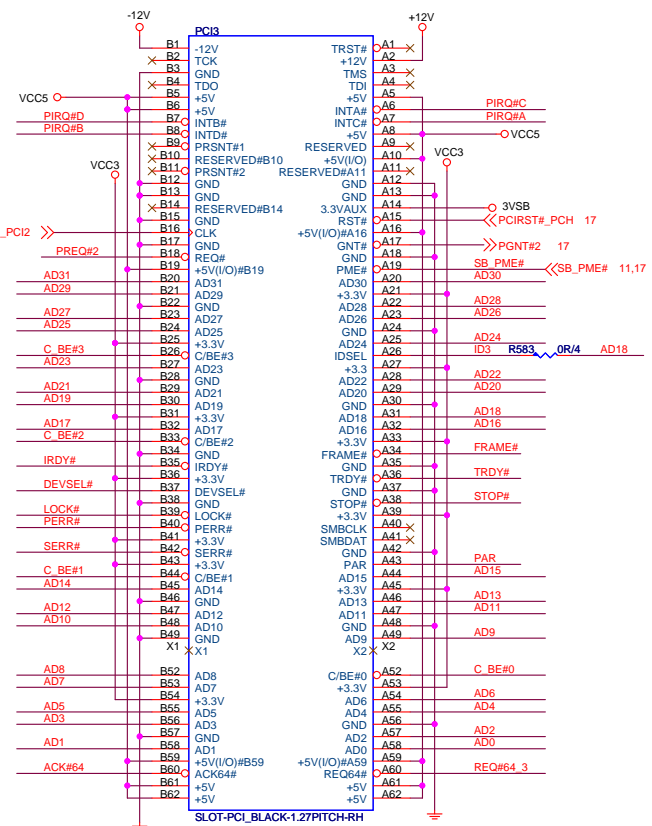
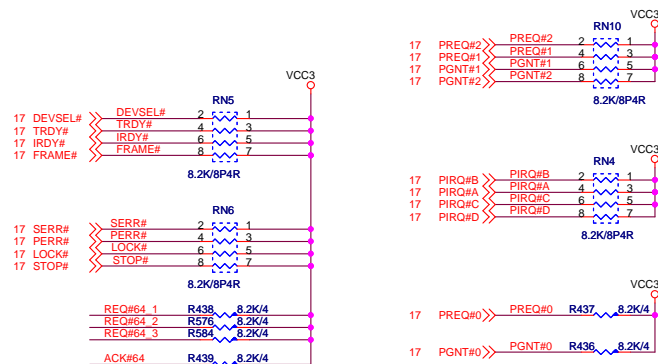
IDSEL = AD16
MASTER = PREQ#0
PIRQ#A

AD[31..0] <<> AD[31..0] 17
C_BE#[3..0] <<> C_BE#[3..0] 17



IDSEL = AD17
MASTER = PREQ#1
PIRQ#B

PCI PULL-UP / DOWN RESISTORS



IDSEL = AD18
MASTER = PREQ#2
PIRQ#C

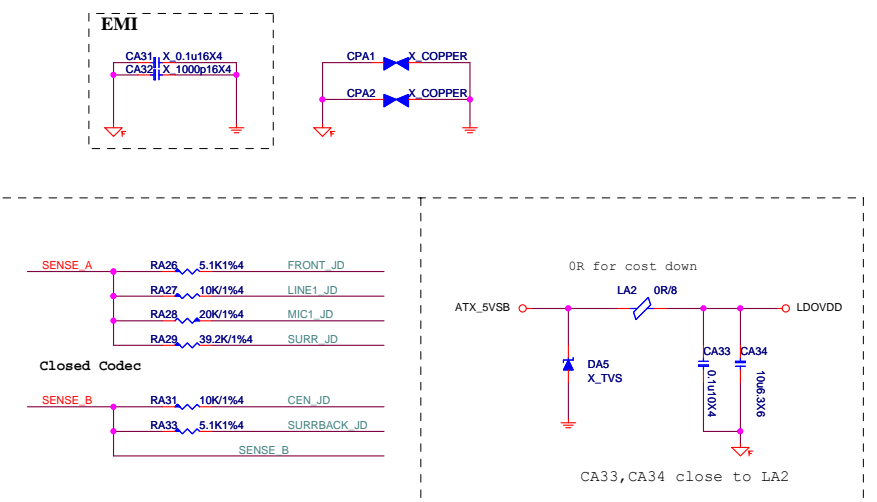
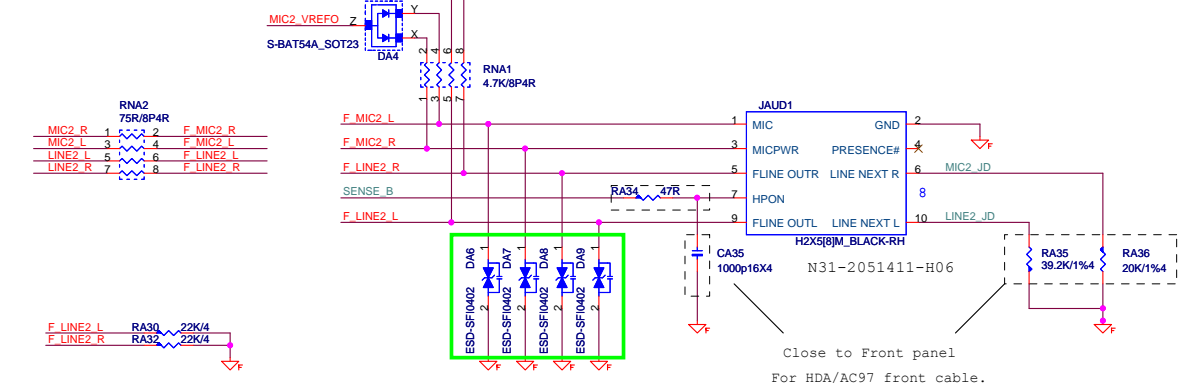
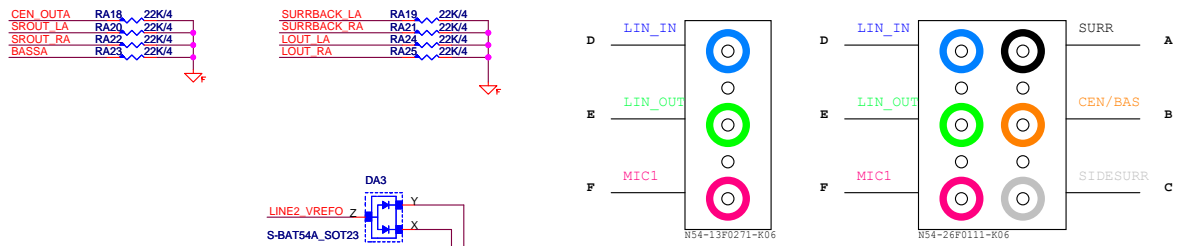
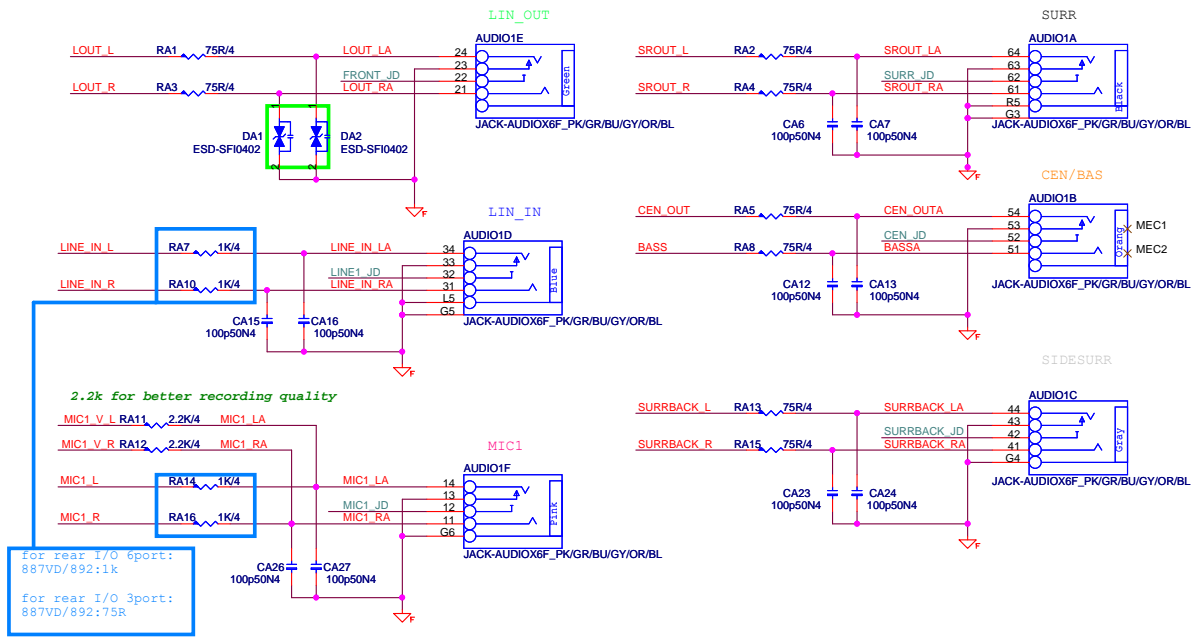
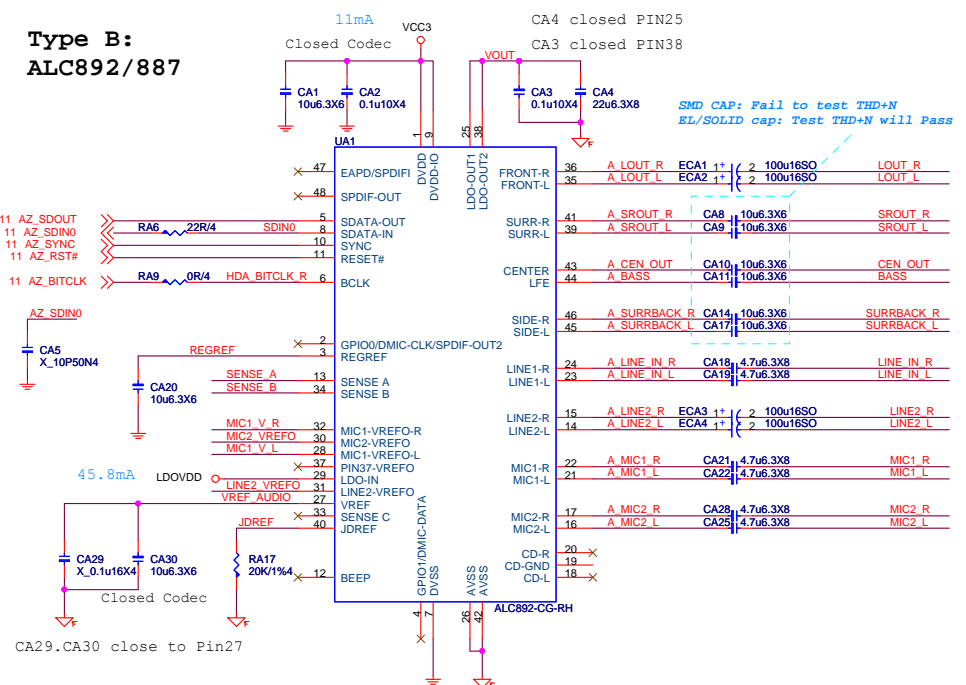
PCI slot (X3)		
+3.3Vaux (wake)	-	1125mA
+3.3Vaux (no wake)	-	60mA
+3.3V	-	7.6A
+5V	-	15A
+12V	-	1.5A



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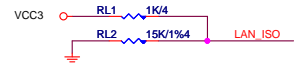
MS-7816

Size	Document Description	Rev
Custom	PCI Slots	12
Date: Tuesday, May 07, 2013		

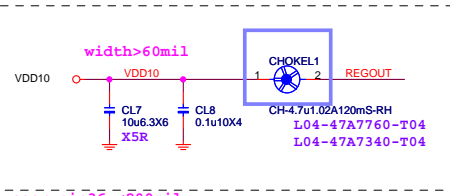


RTL8111E Giga LAN

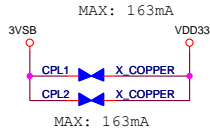
RTL8105E 10/100M LAN



ENSWREG:
1: Enable switching regulator
0: Disable switching regulator



near pin36 <200mil
REFOUT between other signal spacing >15mil

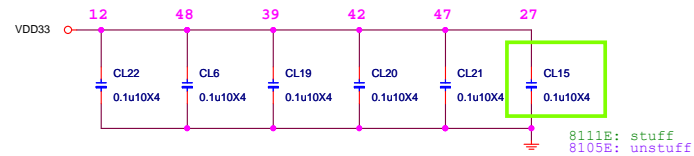


3.3v Power on rise time : 1~100ms.

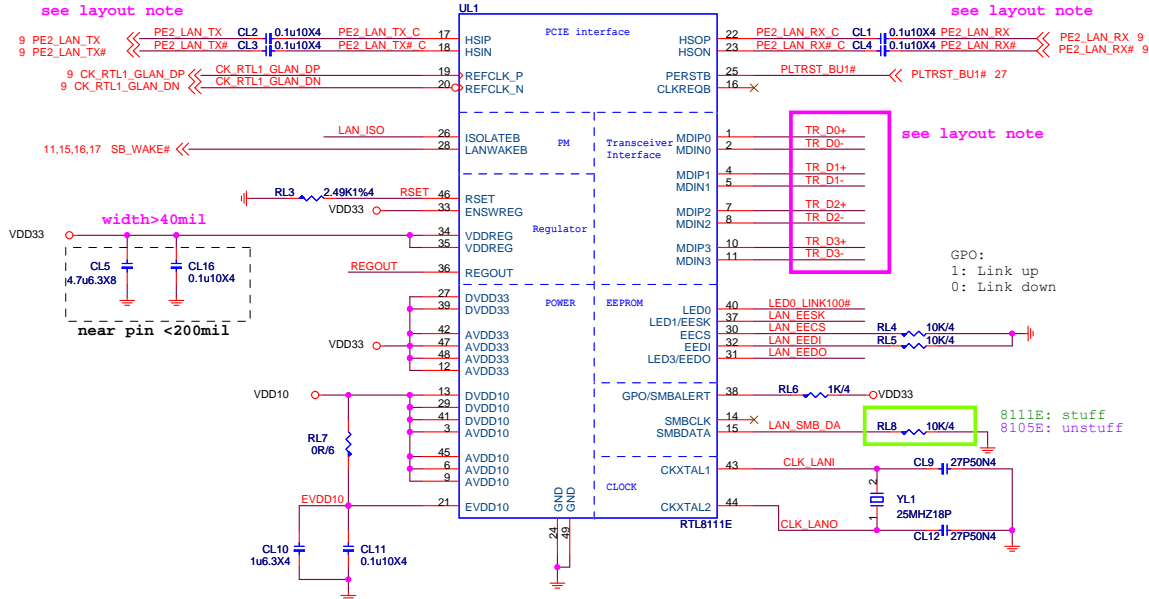
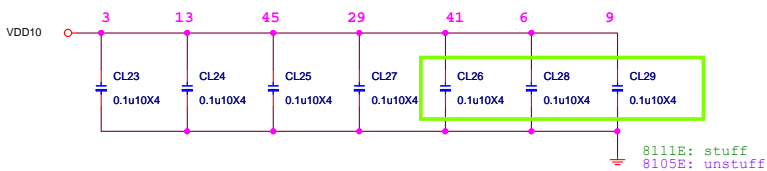
8111E POWER Consumption

	3.3V	mW
10 M Idle/TxRx	12/66	40/218
100 M Idle/TxRx	31/44	102/145
Giga Idle/TxRx	135/163	452/538
ALDPS	4	13

Place near pin

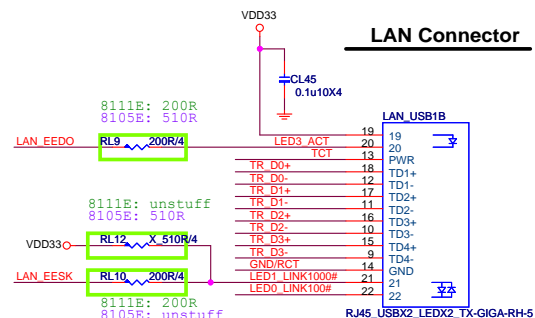


Place near pin

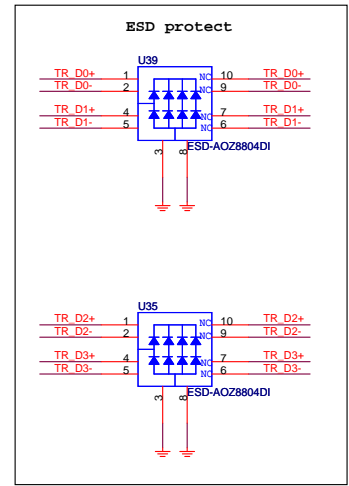
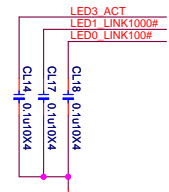


Pin49: 9 via from top layer to GND layer and make the via at the center of IC.

LAN Connector

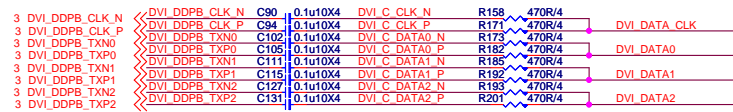


only support LED0+LED1/LED1+LED3 dual color LED combinations when using EEPROM

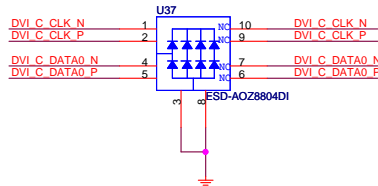


Giga-Lan	10/100-Lan
N58-22F0731 Link Yellow Active Blinking 1000 Orange 100 Green 10 None	N58-22F0771 Link Yellow Active Blinking 100 Green 10 None
19 20 21 22	19 20 21 22

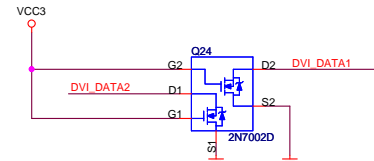
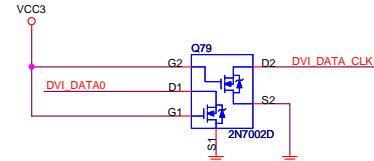
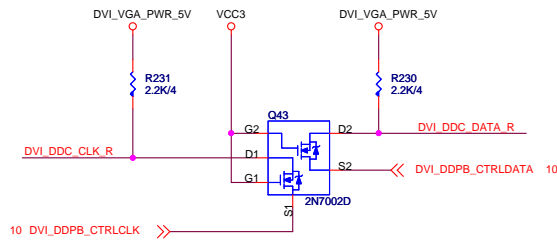
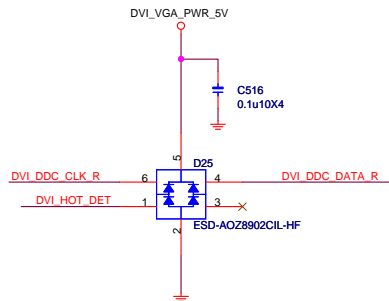
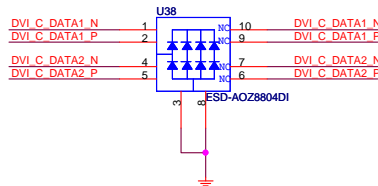
VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)



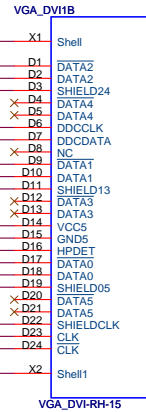
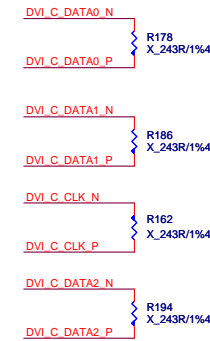
U26 AVL:D0G-05A050C-005
D0G-06A050C-A68



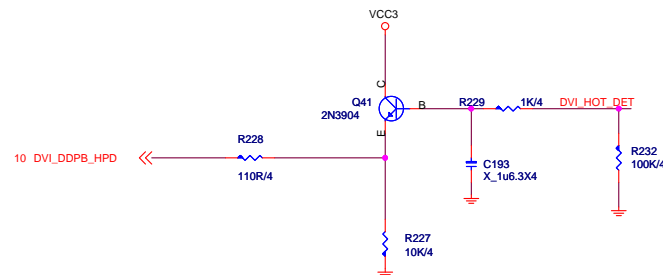
U27 AVL:D0G-05A050C-005
D0G-06A050C-A68



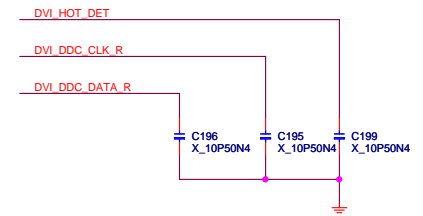
For EMI



HPD



EMI

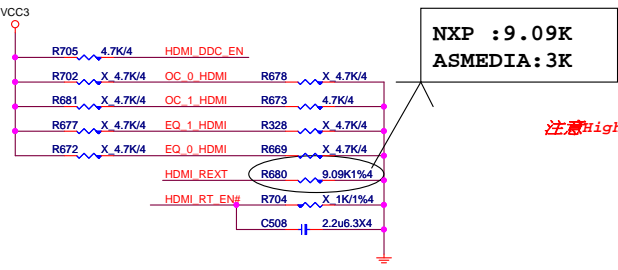
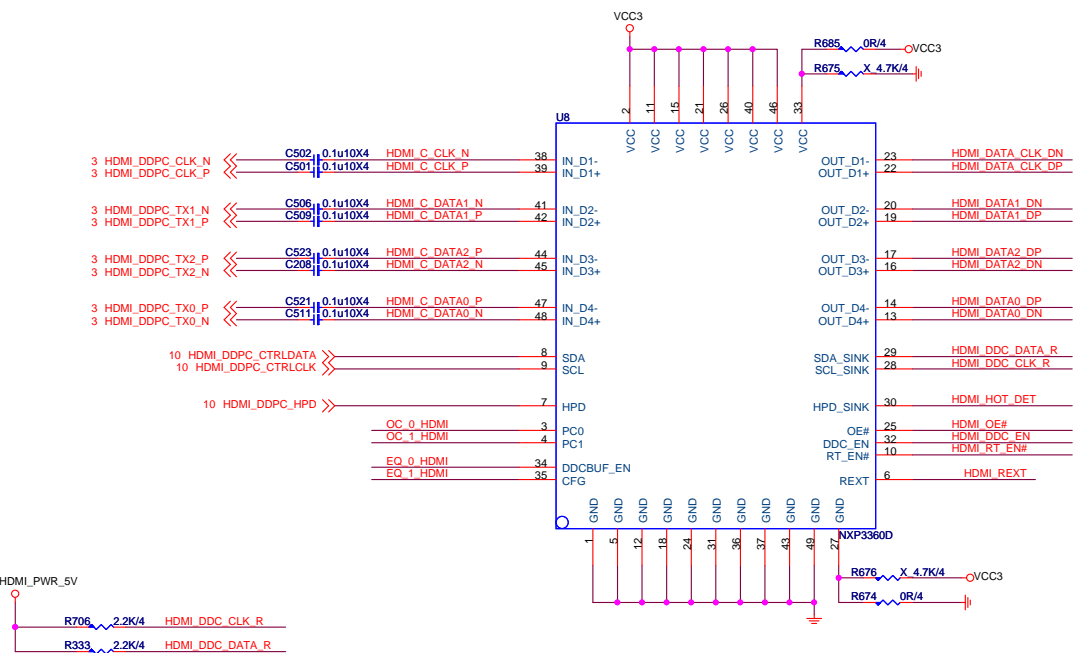


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HDMI level shifter

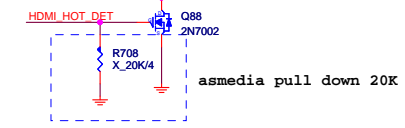


	"0"	"1"
DDC_EN	DDC level shifter disable	DDC level shifter enable
RT_EN#	Input 50 ohm termination resistor enable	the input termination ; resistors are set to high impedances
OE#	enable	the chip is power down and input termination resistors will be at high impedance.
HPD_SINK	disable	enable
DDCBUF_EN	For DDC level shifting configuration, please refer to Table.	
REXT		

[DDC_EN, DDCBUF_EN, OE#]	DDC Passive Switch	DDC Active Buffer
1, 0, X	On	Off
1, 1, 0	Off	On
1, 1, 1	Off	Off
0, X, X	Off	Off

PC1, PC0		note
00	8 dB	internal pull-down at ~500K ohm.
01	4 dB	
10	12 dB	
11	0 dB	

注意High/Low Detect



note
internal pull-up at ~500K ohm.
internal pull-down at ~500K ohm.
internal pull-down at ~500K ohm.
internal pull-down at ~200K ohm; 5V tolerant.
internal pull-down at ~500K ohm.
analog current generation.

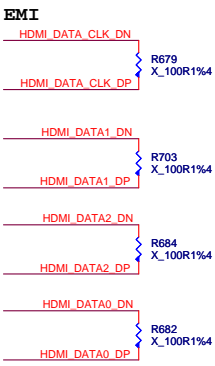
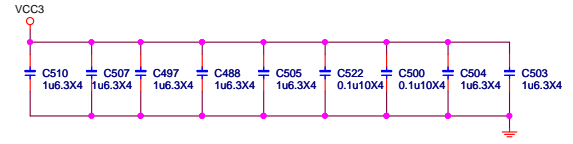
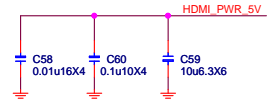
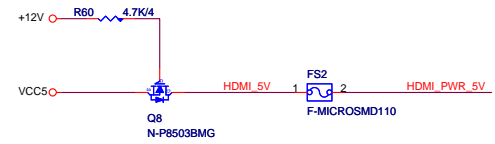
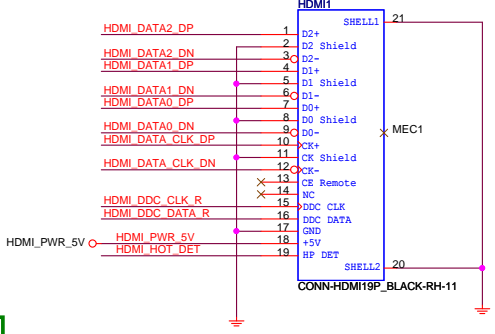
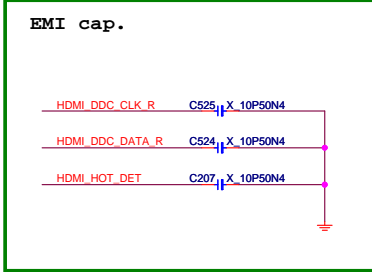


Table 8-1. PCH PCI Express Tx/RX - HDMI Signal Mappings

Port	Digital Display Interface Differential Pairs	HDMI Signals	PCH Digital Display Interface Pins
Port B	DDSP_B_TX0_DN	TMDSPB_DATA2#	DDPB_ON
	DDSP_B_TX0_DP	TMDSPB_DATA2	DDPB_OP
	DDSP_B_TX1_DN	TMDSPB_DATA1#	DDPB_1N
	DDSP_B_TX1_DP	TMDSPB_DATA1	DDPB_1P
	DDSP_B_TX2_DN	TMDSPB_DATA0#	DDPB_2N
	DDSP_B_TX2_DP	TMDSPB_DATA0	DDPB_2P
	DDSP_B_TX3_DN	TMDSPB_CLK#	DDPB_3N
	DDSP_B_TX3_DP	TMDSPB_CLK	DDPB_3P
	DDPB_HPD	DDSP_B_HPD0	Hot plug detect used by HDMI Port B. HDMI DDC lines for Port B
	SDVO_CTRLCLK	HDMIB_CTRL_CLK	
	SDVO_CTRLDATA	HDMIB_CTRL_DATA	



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Size CustomDocument DescriptionHDMI Connector

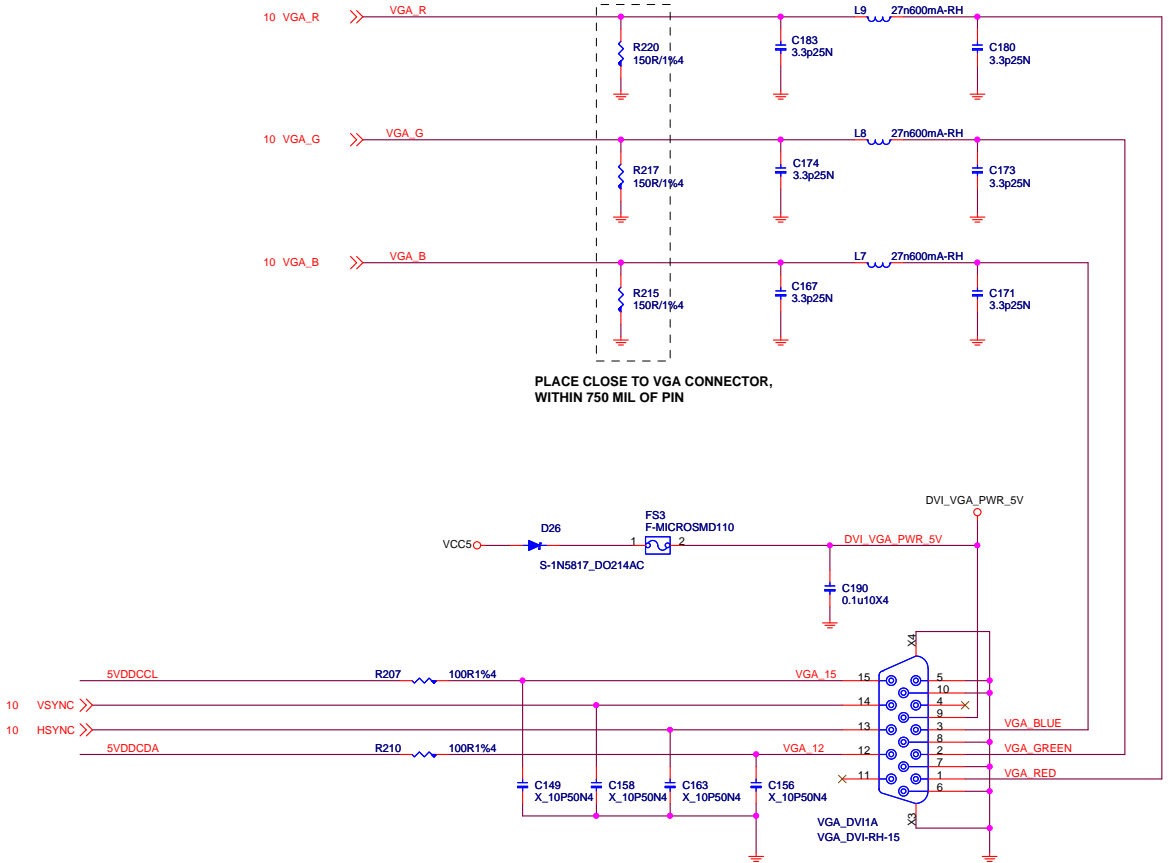
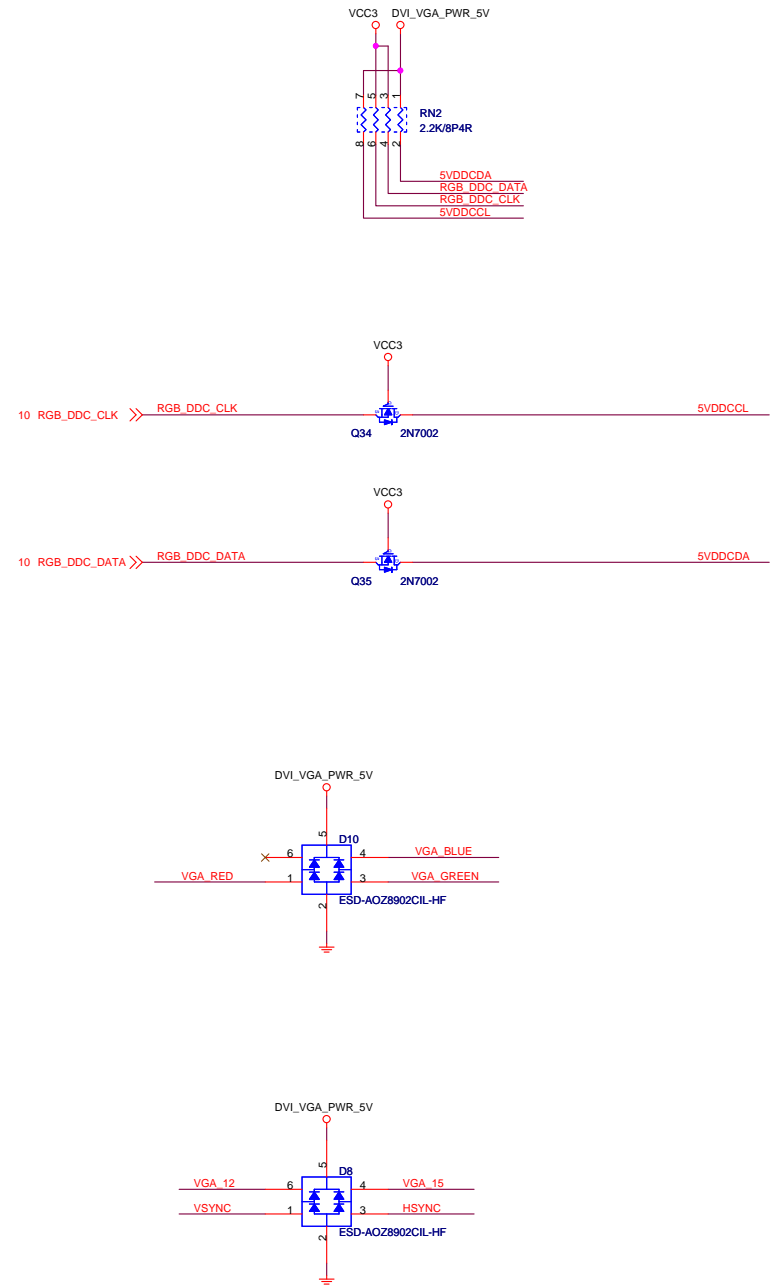
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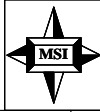
D-Sub

VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)

Level shift



PLACE CLOSE TO VGA CONNECTOR,
WITHIN 750 MIL OF PIN



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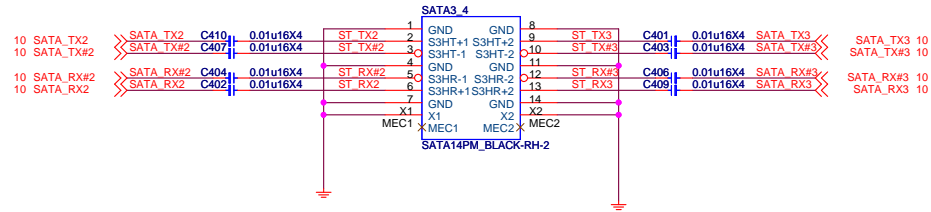
SATA 6G PORT 0,1

3.0 BLACK



SATA 3G PORT 2,3

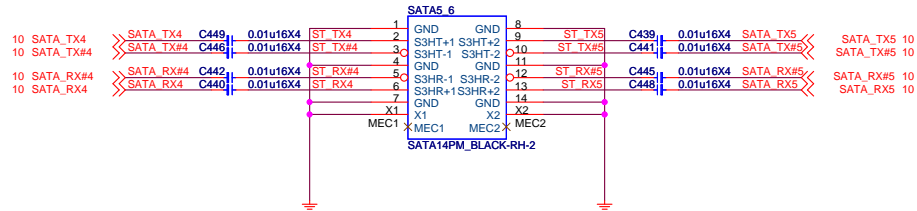
3.0 BLACK



SATA 3G PORT 4,5

Z87,H87 chip support SATA3.0
B85 chip support SATA2.0

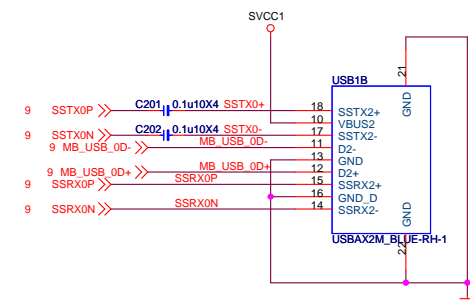
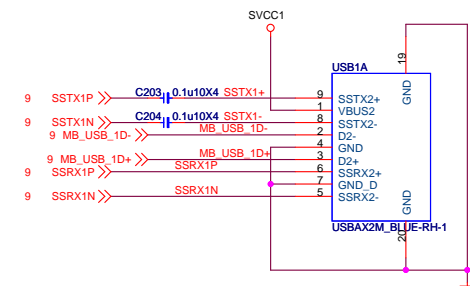
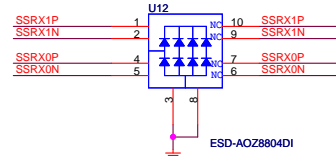
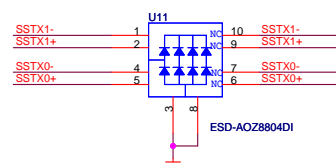
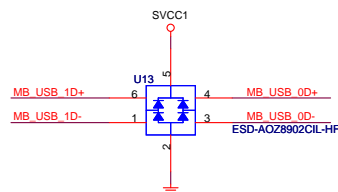
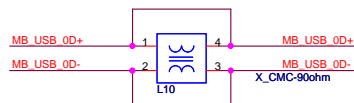
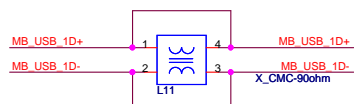
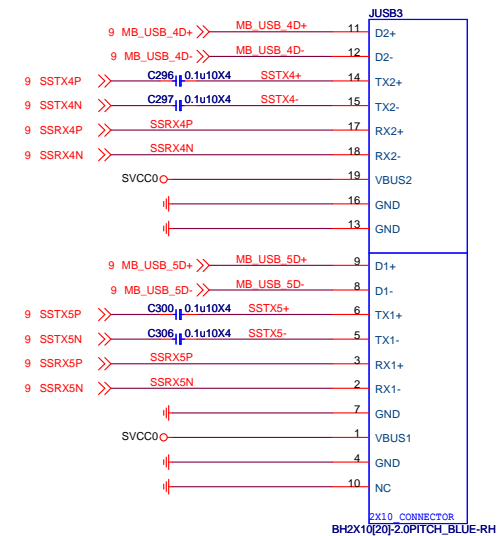
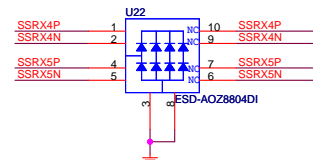
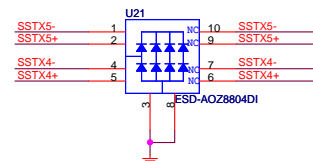
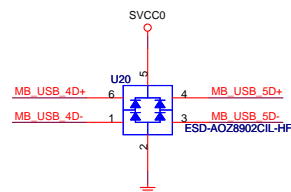
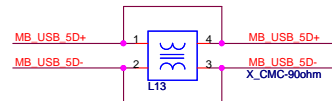
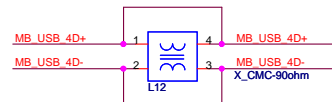
3.0 BLACK



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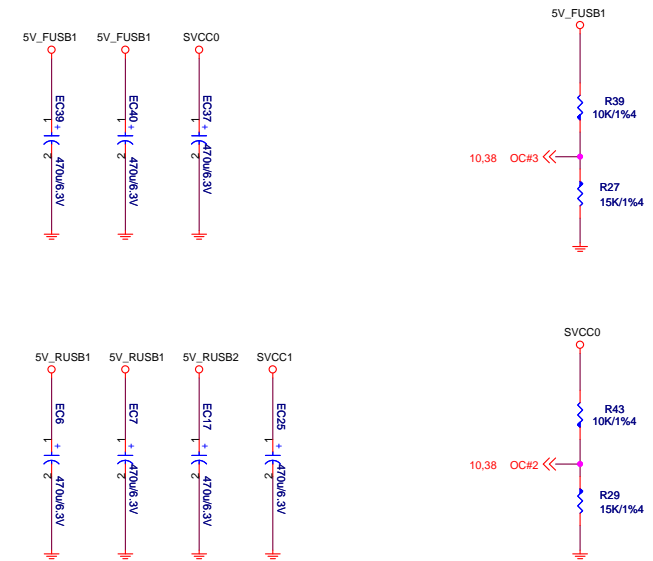
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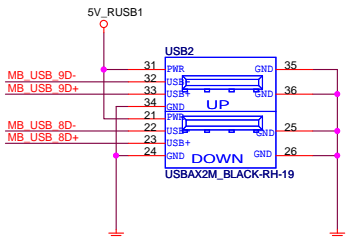
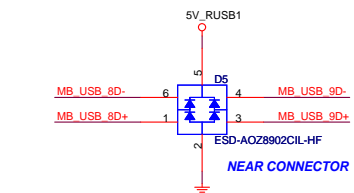
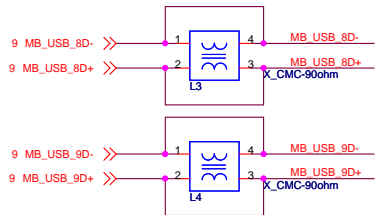
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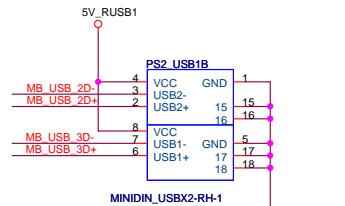
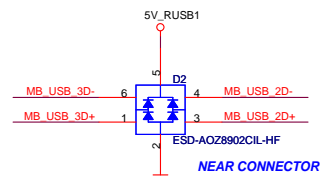
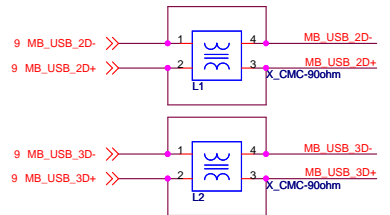


5VDRV1, 5VSBDRV1 width 12mil
D08-0300700-P16 (Itrip=2.6A; 0.015ohm) support 2 USB ports

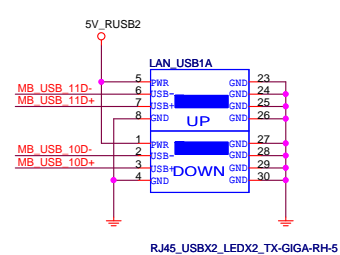
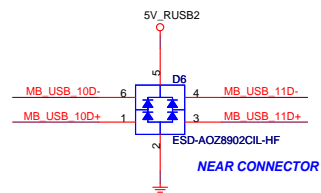
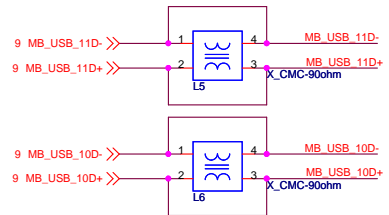
REAR USB PORT 2,3



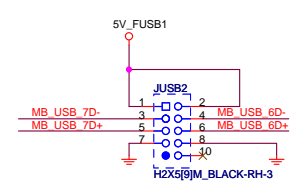
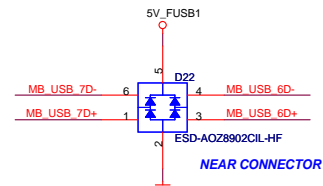
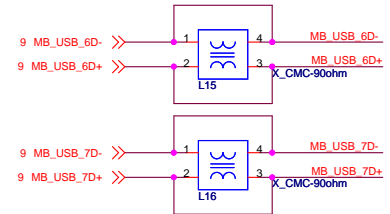
REAR USB PORT 8,9 (With PS2)



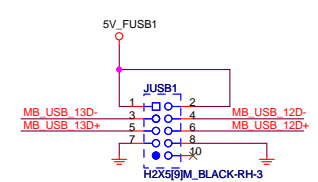
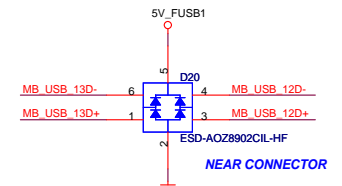
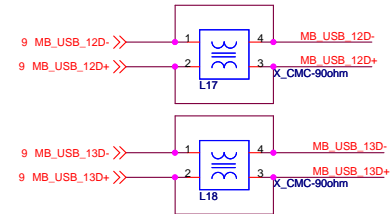
FRONT USB PORT 10,11 (With LAN)



FRONT USB PORT 6,7



FRONT USB PORT 12,13

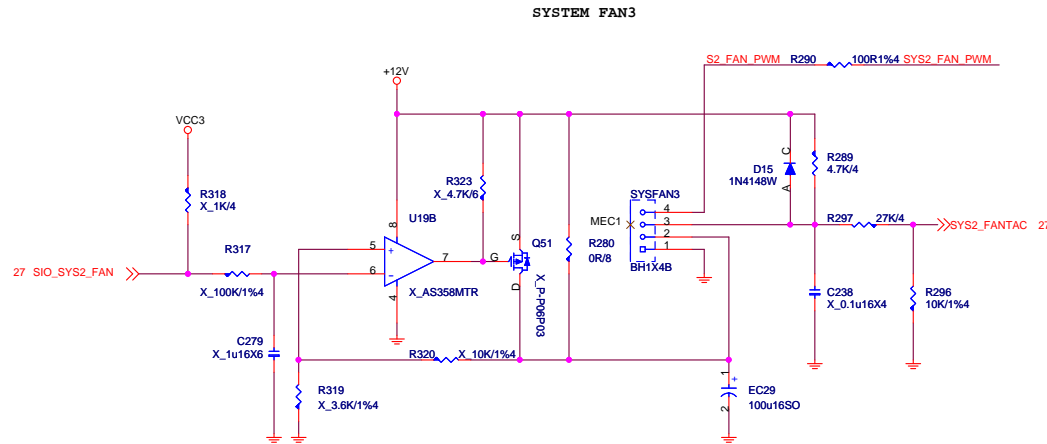
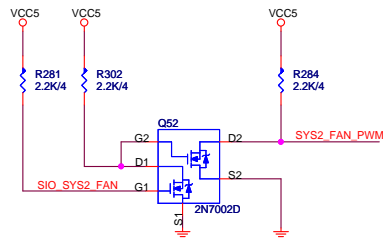
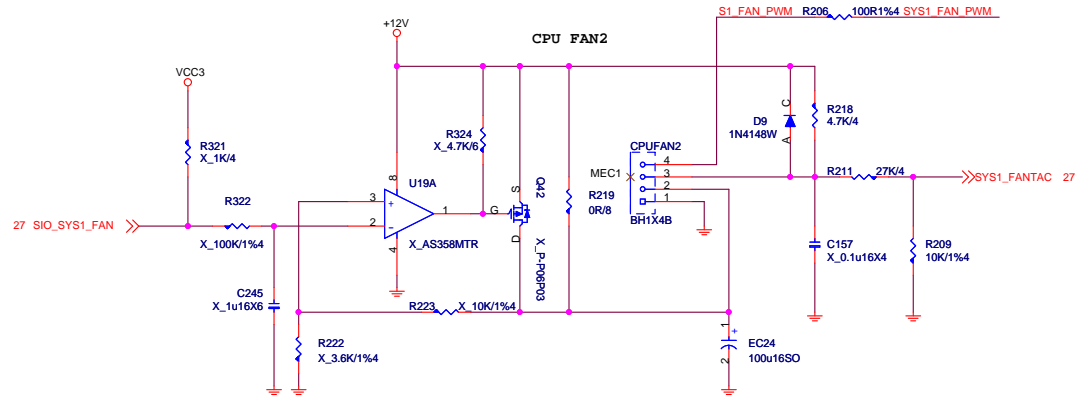
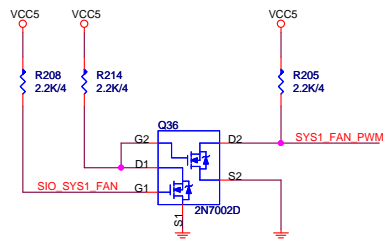
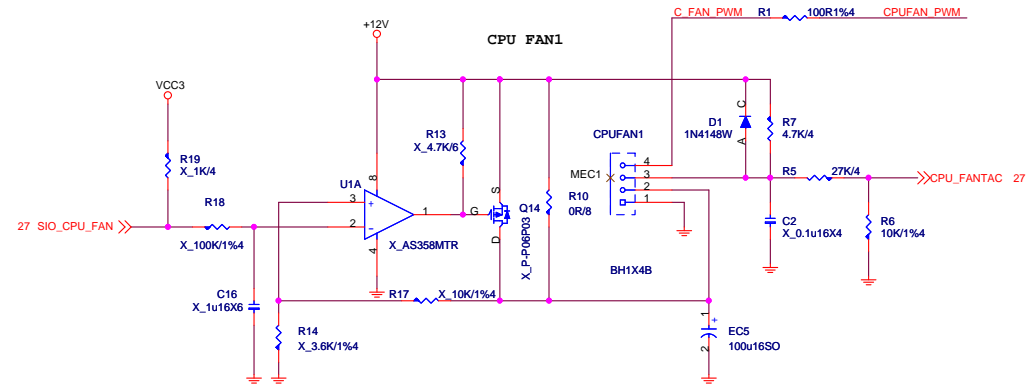
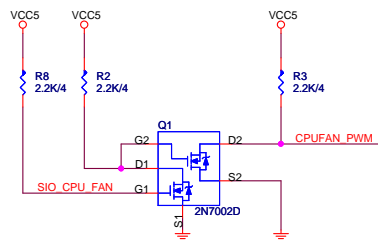


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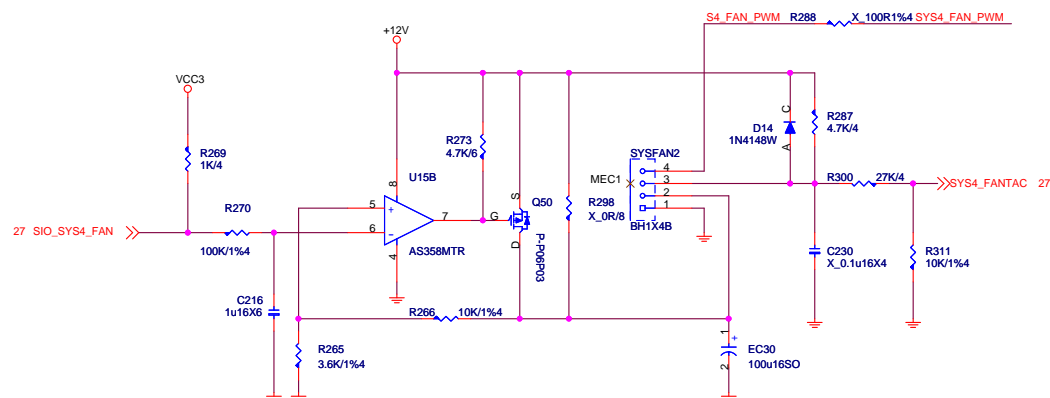
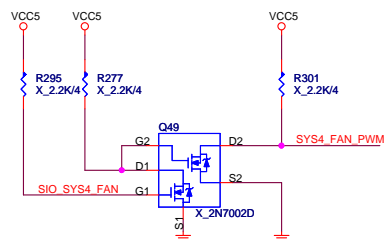
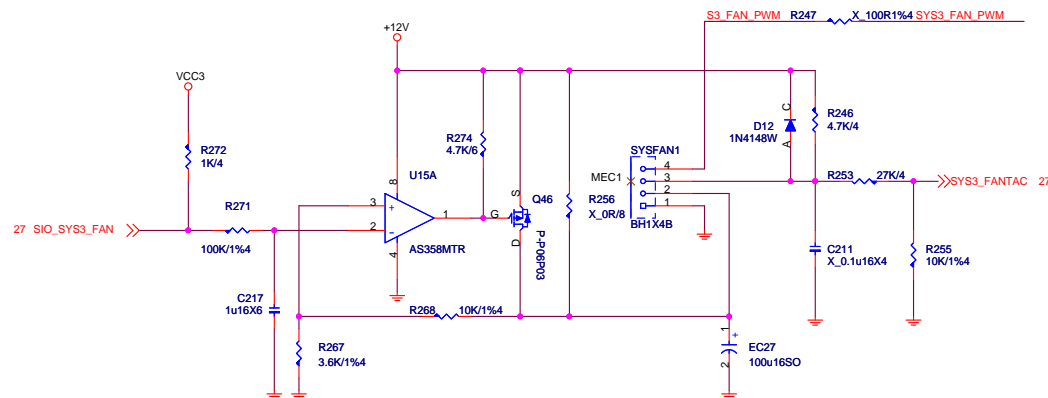
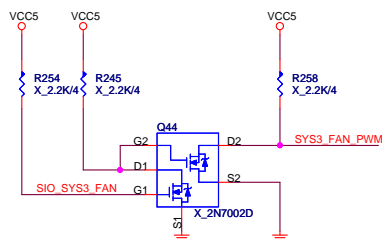
FAN-COUNTROL CIRCUIT



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K4[7]



D



B



B



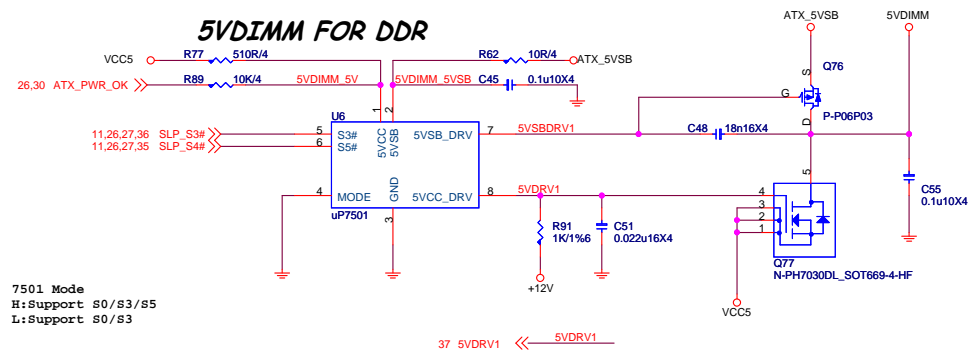
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Document Description	Rev
ATX F Panel/EMI/TPM	12

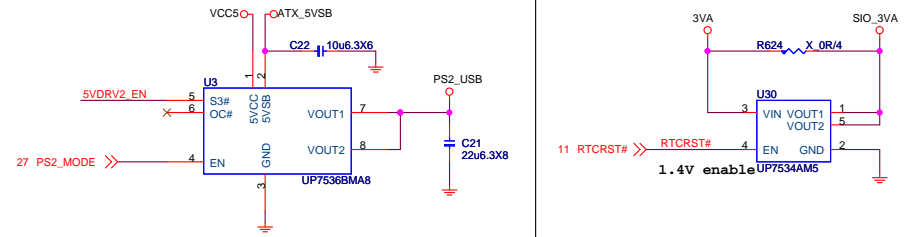
Sheet 30 of 44

Rev
12

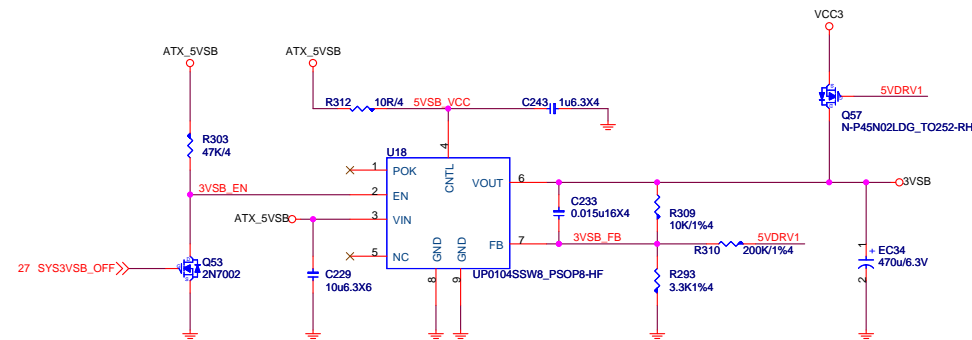
5VDDIMM FOR DDR



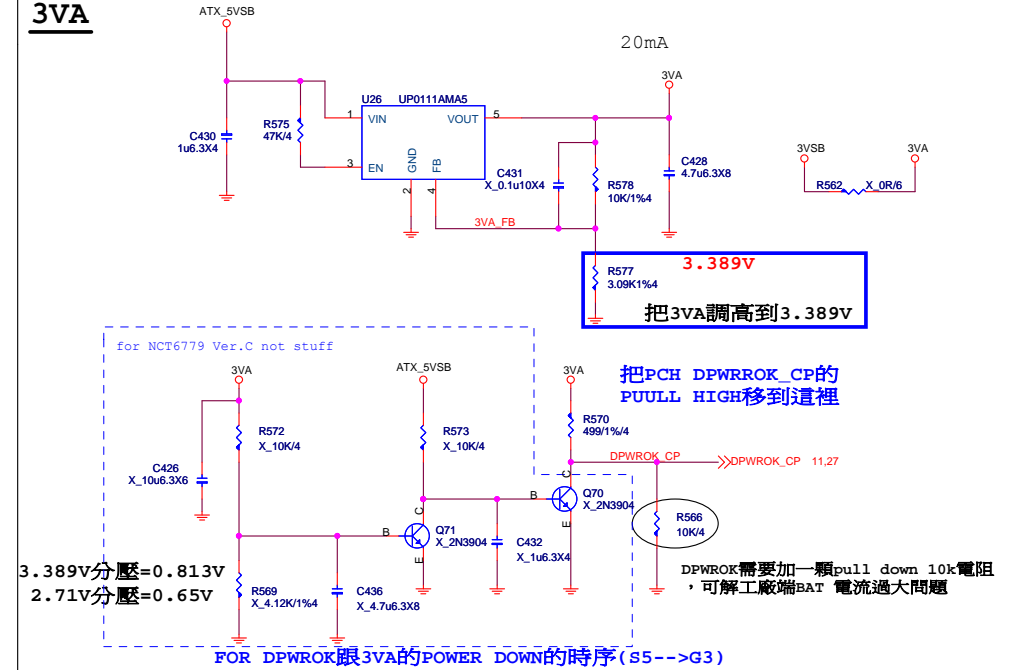
PS2 Power



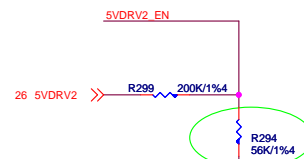
3VSB



3VA

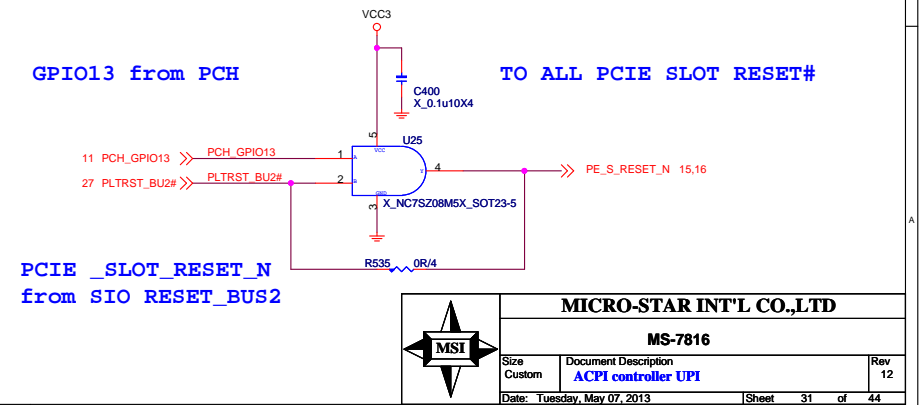


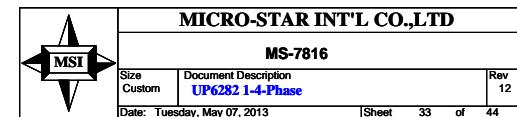
USB MODE

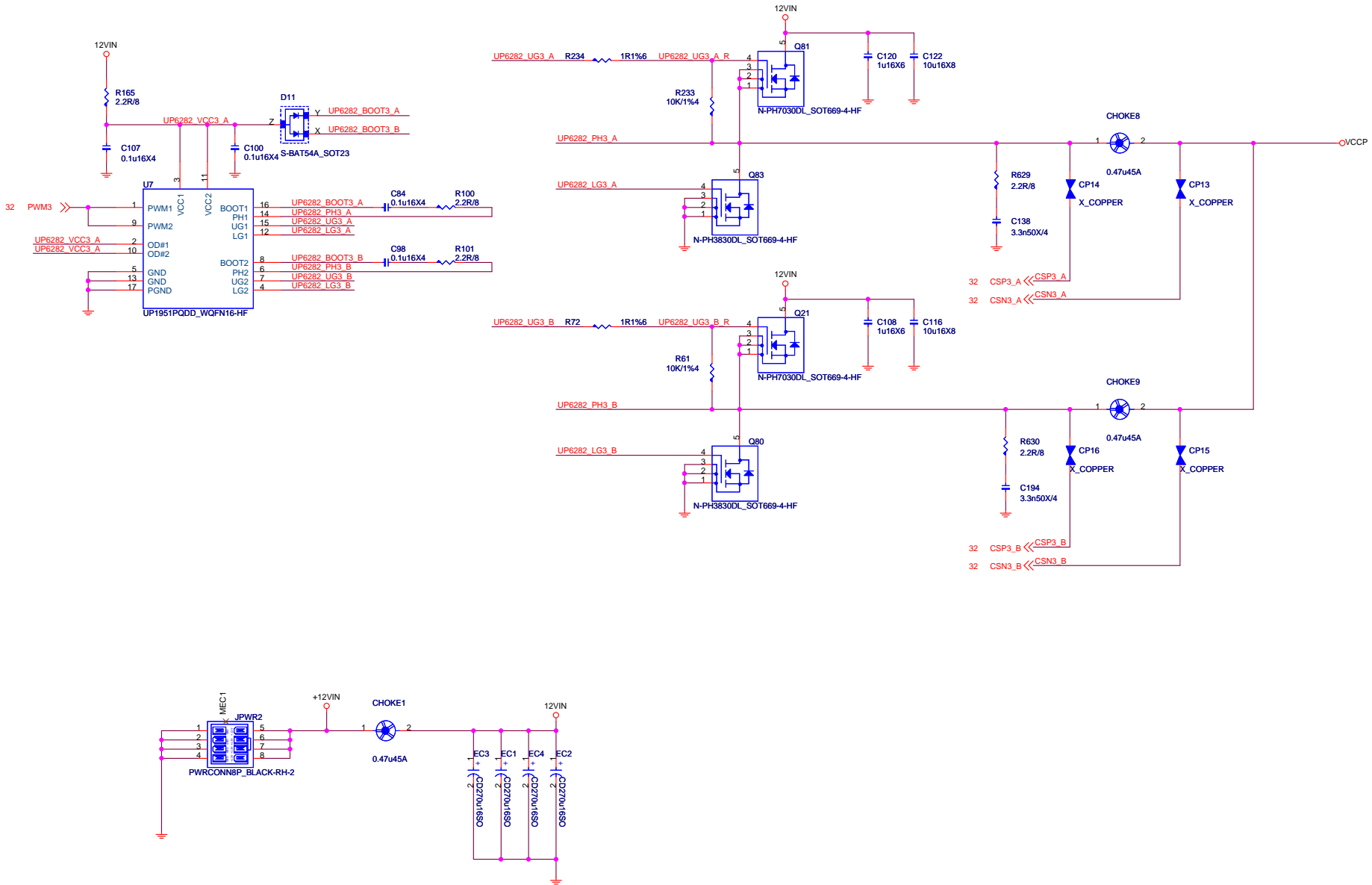


GPIO13 from PCH

TO ALL PCIE SLOT RESET#







DDR Power:1.5V

DDR3_1.5V 4.2A+12A+1.115A+6A=23.315A

4.2A FOR CPU

12A FOR 4DIMM

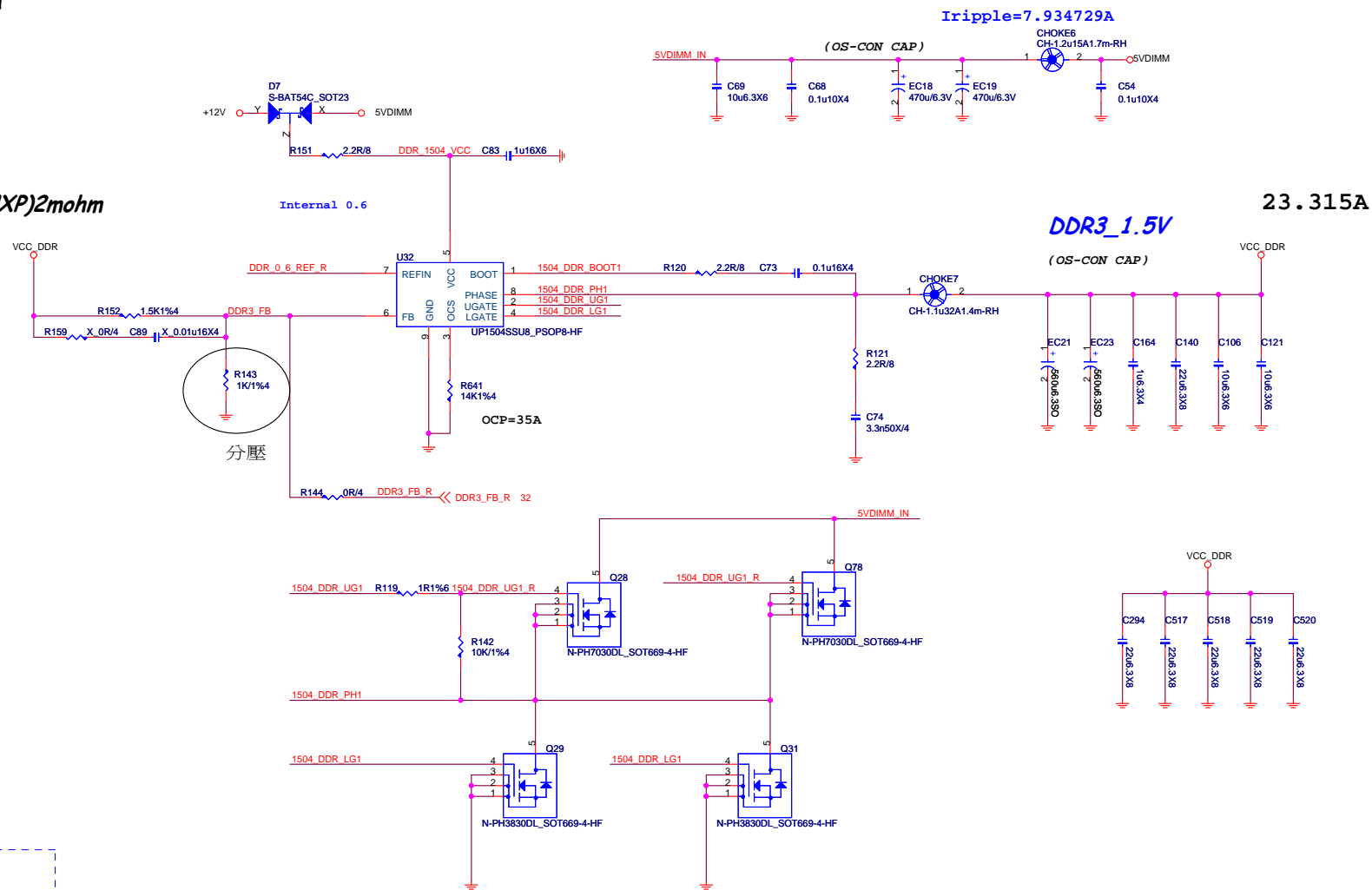
1.115A FOR VTT_DDR

PCH Core 6A

OCP 23.315A*1.5=34.9725A

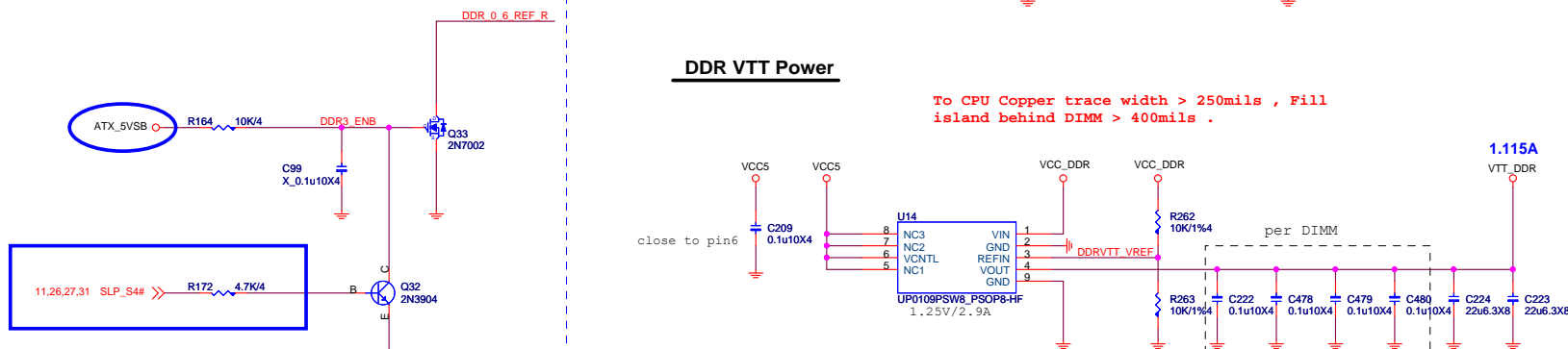
OCP=[20uA*Rocs(R320)]/4*Rdson(Low side NXP)2mohm

R320=14K ohm



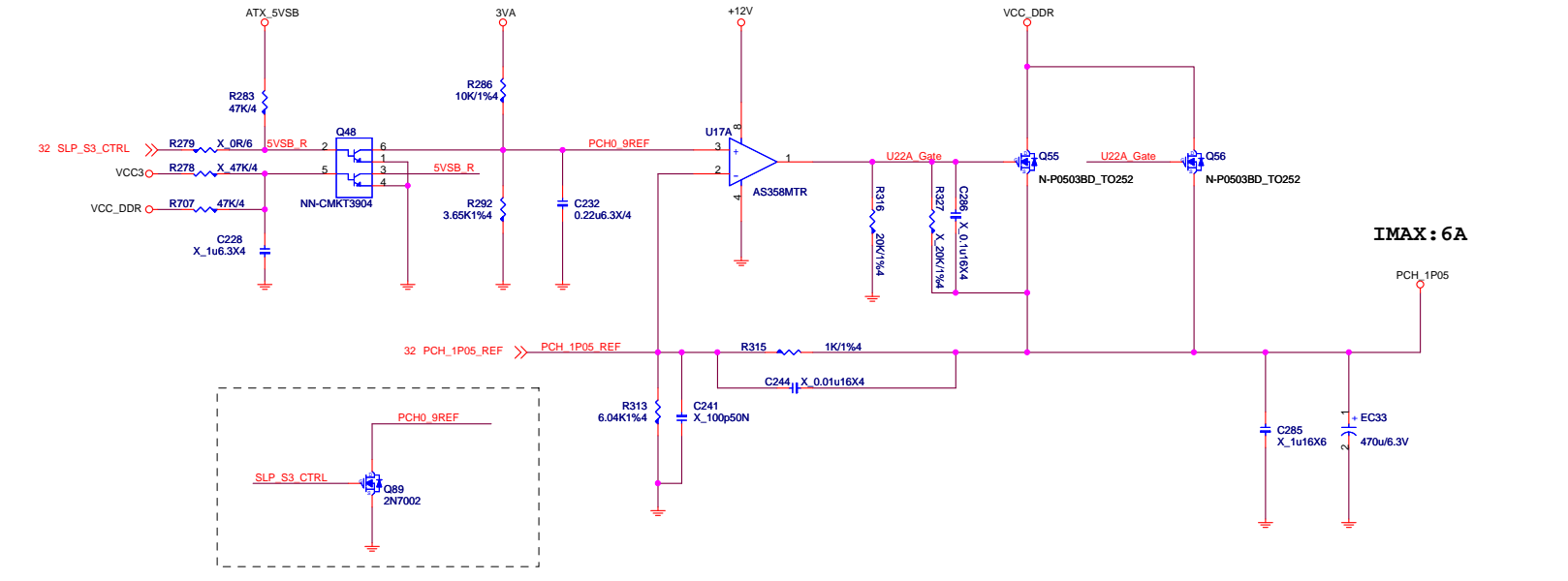
DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .

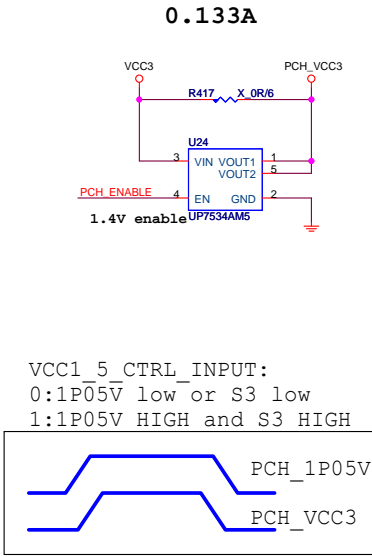


P.S. Only for meet Intel power down sequence.

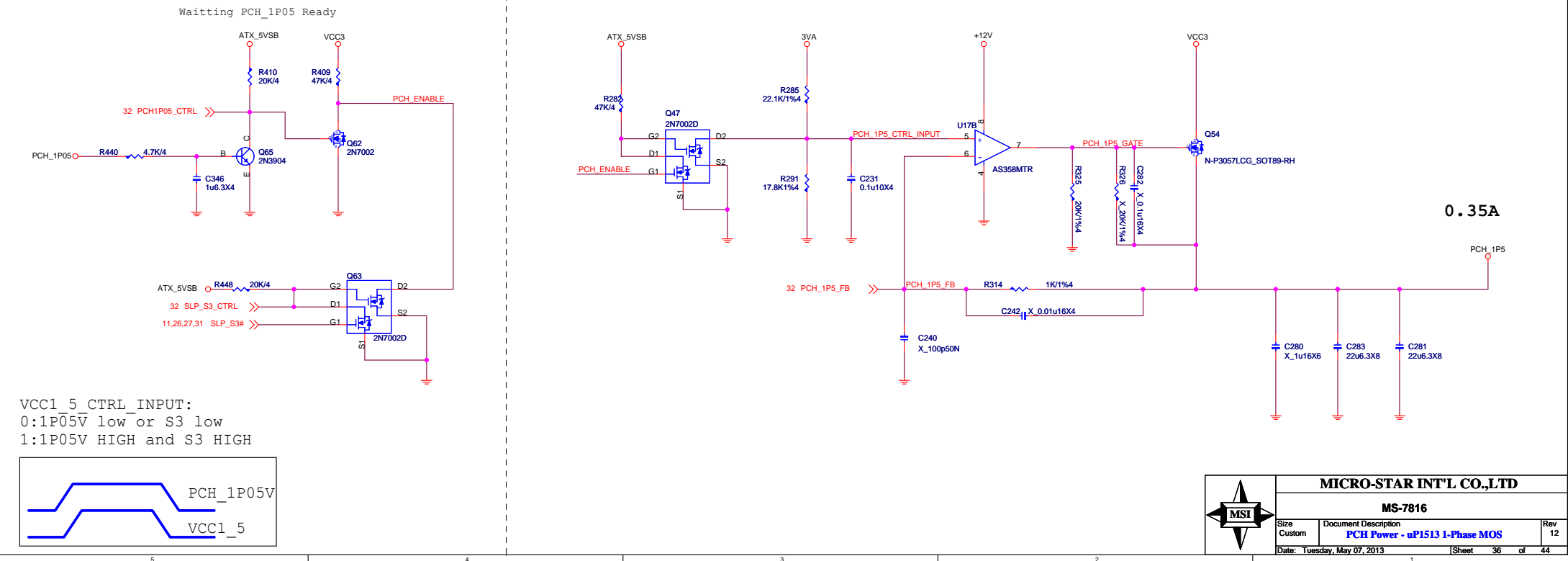
PCH Power:1.05V
PCH Core 6A



PCH Power:3.3V



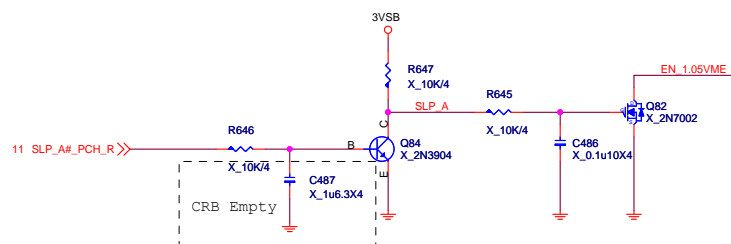
PCH Power:1.5V



C318,C323,R378,C313,C314,C333,R366 for H87 un stuff
Z87 only stuff R354

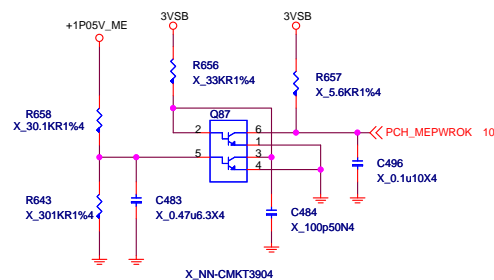
SLP_A

ME Power Control



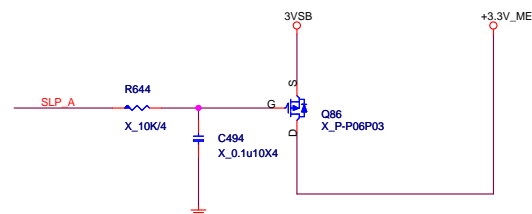
SLP_A#_PCH_R R666 X_0R/4 EN_1.05VME

PCH_MEPWROK

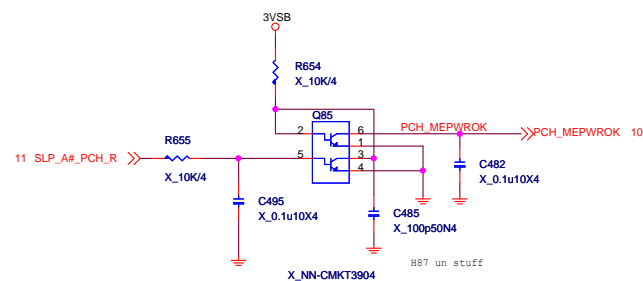
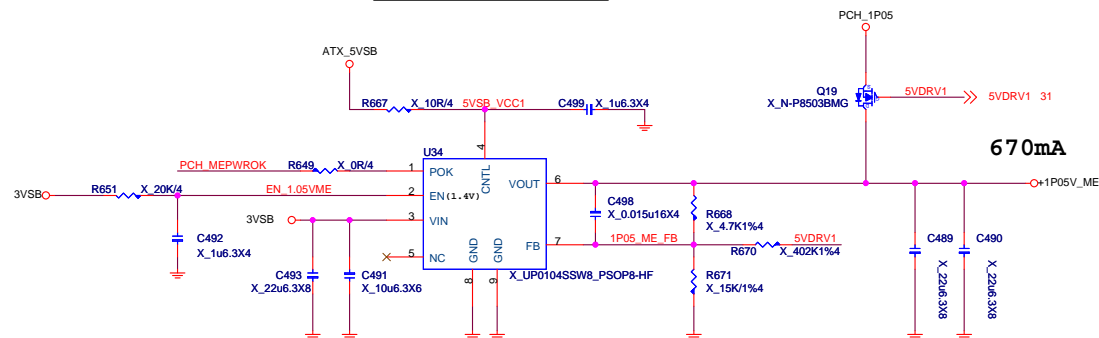


VccASW active to APWROK high lms

+3.3V_ME



+1.05V_ME(VCCIO_ME)



APWROK falling to VccASW falling 40ns

For INTEL ME BUG

Z87->Stuff R653
H87->Stuff R652

+3.3V_ME R652 X_0R/6 SPI_VCC3
VCC3 R653 0R/6

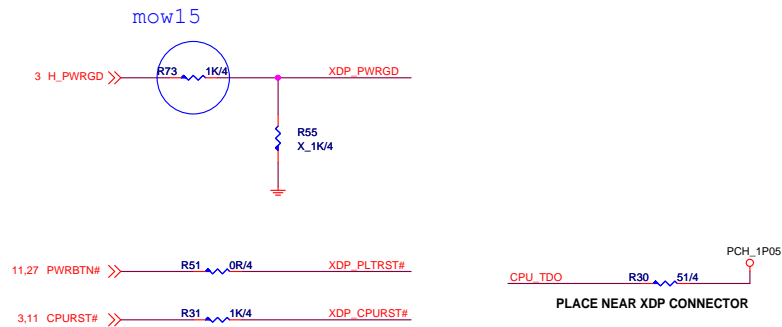
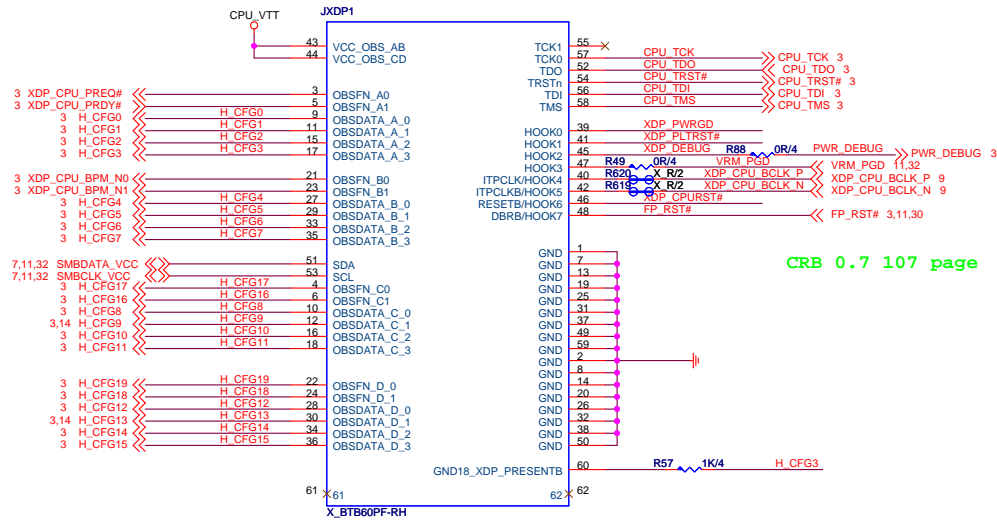


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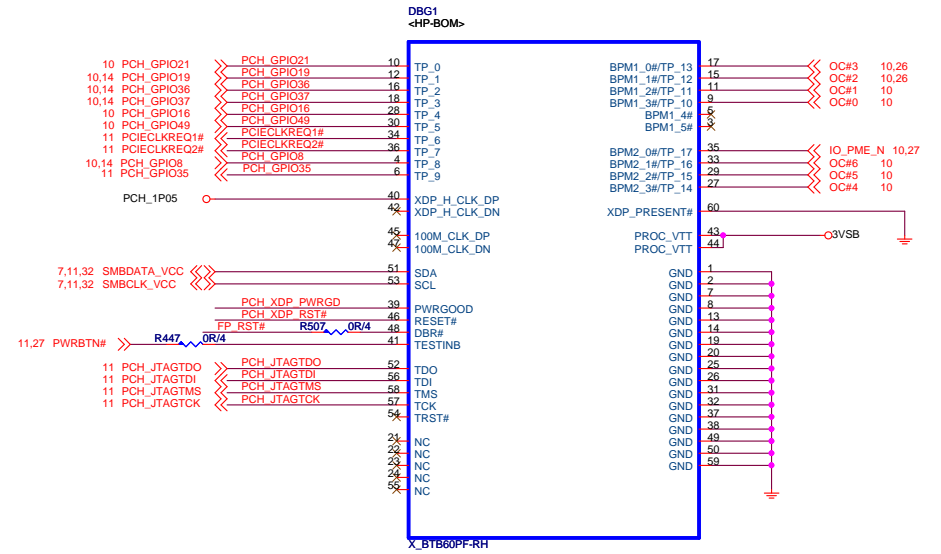
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Reserve debug port 5020



PCH XDP



PCH XDP PWRGD/RESET

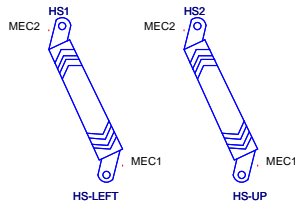
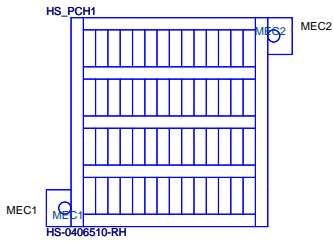




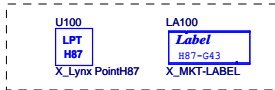
2013/3/112013/3/18PK0-0781612-G37,精成,25,寶安恩斯邁廠(MSIS)4,Coffee
2013/3/112013/3/18PK0-0781612-G37,精成,200,寶安恩斯邁廠(MSIS)4,Coffee
2013/3/112013/3/18PK0-0781612-E48,競華,25,寶安恩斯邁廠(MSIS)4,Coffee



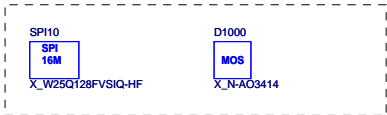
HEATSINK



H87 OPT.



SPI OPT.



Z87 OPT.



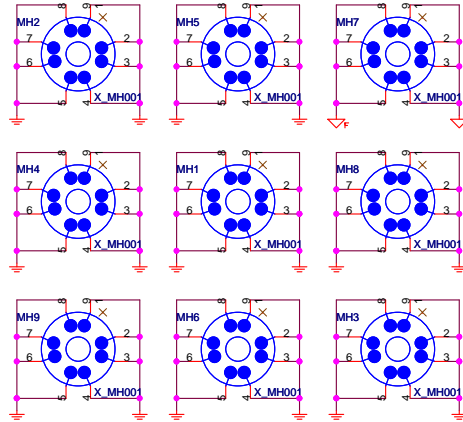
B85 OPT.



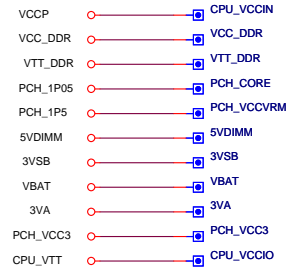
ZH87 OPT.



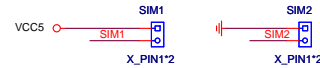
Mounting Holes



Test point



Simulation



Optical Fiducial Marks-120

